MEGAHUNT

MH1721
Brief Introduction

Highly Integrated Secure SOC

Version: 1.5
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Megahunt Tehnologies Inc.

History of Revision

Date	Version	Description	Author
2021-01-06	1.00	Completed the first draft	MEGAHUNT
2021-03-05	1.10	Updated package information	MEGAHUNT
2021-03-12	1.20	Updated electrical parameters	MEGAHUNT
2021-06-30	1.30	Deleted QFN32,DFN8 package	MEGAHUNT
2021-11-15	1.40	Updated SOP8, QFN16_SE PIN definition	MEGAHUNT
2021-12-19	1.50	Added ordering information	MEGAHUNT

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1 Overview

1.1 Description

The MH1721 has internal 32-bit RISC processor with up to 80MHz frequency.

MH1721 has built-in symmetric algorithm encryption engine SCP (supports symmetric encryption algorithms such as DES/AES), asymmetric encryption co-processor ASCP (supports asymmetric algorithms such as RSA/ECC), and also supports Hash algorithms such as SHA160/224/256/384/512. In addition, in order to improve safety and reliability, MH1721 provides various detection mechanisms such as voltage, frequency, temperature, light, voltage glitch, MESH, and tamper-proof.

MH1721 supports MPU (memory protection unit), which can control the access authority to the memory.

MH1721 has built-in 16KB RAM, 256KB FLASH, and integrates various communication interfaces such as USB, SPI, UART, I2C, 7816 Slave, etc. All peripheral driver software is compatible with the current mainstream security chip software interfaces.

1.2 Main functions and characteristics

- 32-bit RISC processor
  - MPU memory protection unit
  - Maximum 80MHz main frequency
  - Support Privilege and unprivileged two operating states
  - Low power consumption design
- Memories
  - 16KB RAM
  - 256KB FLASH
    - Support page erasing and writing
    - More than 500,000 times of repeated erasing and rewriting, 10-year data retention
    - Page (512B) erasing time 50us
    - Writing 256 bytes time 400us
    - Full erasing time 15ms
- System control module (controls all peripheral module clocks and system-related configurations)
- Security encryption algorithm Co-processor
  - ASCP Co-processor
    - Support 512~4096 bits (integer multiple of 64) RSA operation,and support

anti-SPA/DPA/FA/DFA function

- Support anti-SPA/DPA/FA/DFA function
- Support 192/224/256/384/521 bits ECC operation, support anti-SPA/DPA/FA/DFA function

- DES/AES Co-processor
  - Support DES/3DES ECB/CBC mode operation
  - 3DES algorithm supports 2-KEY method
  - Support anti-SPA/DPA/FA/DFA attack design

- 1 UART interface (support 4-wire)
- 1 SPI interface (master and slave can be configured)
- 1 I2C interface
- 1 7816 Slave interface
- 4 32-bit TIMER
- Integrated internal watchdog
- 1 random number generator including true/pseudo-random number generation
- 1 DMA controller (supports 2-channel DMA transfer)
- 1 CRC module
- Support up to 8 GPIOs
- Internal environment monitoring Sensor (high and low voltage, high and low temperature, MESH, clock, light and voltage glitch detection)
- Support 4-way Tamper (dynamic and static configurable, internal integrated 7.5MΩ resistance)
- 1 USB1.1 Device, support full speed
- Integrated LDO that can output 70mA drive capability

1.3 Applications

USB KEY, data encryption and decryption, authentication, key negotiation, IP protection, IoT terminals authentication, etc.

1.4 Package Types

- QFN16
- DFN10
- SOP8

1.5 Description of the infrastructure

MH1721 has internal 32-bit RISC processor, 16KB RAM, 256KB Flash, system control module, security encryption module, TRNG(true random number generator), one DMA controller, 1 USB interface, 1 GPIO module, 1 WDT module, 4 32-bit Timers, 1 CRC module, 1 SPI interface, 1 UART interface, one 7816 Slave interface, and one I2C interface. The

block diagram is as follows:

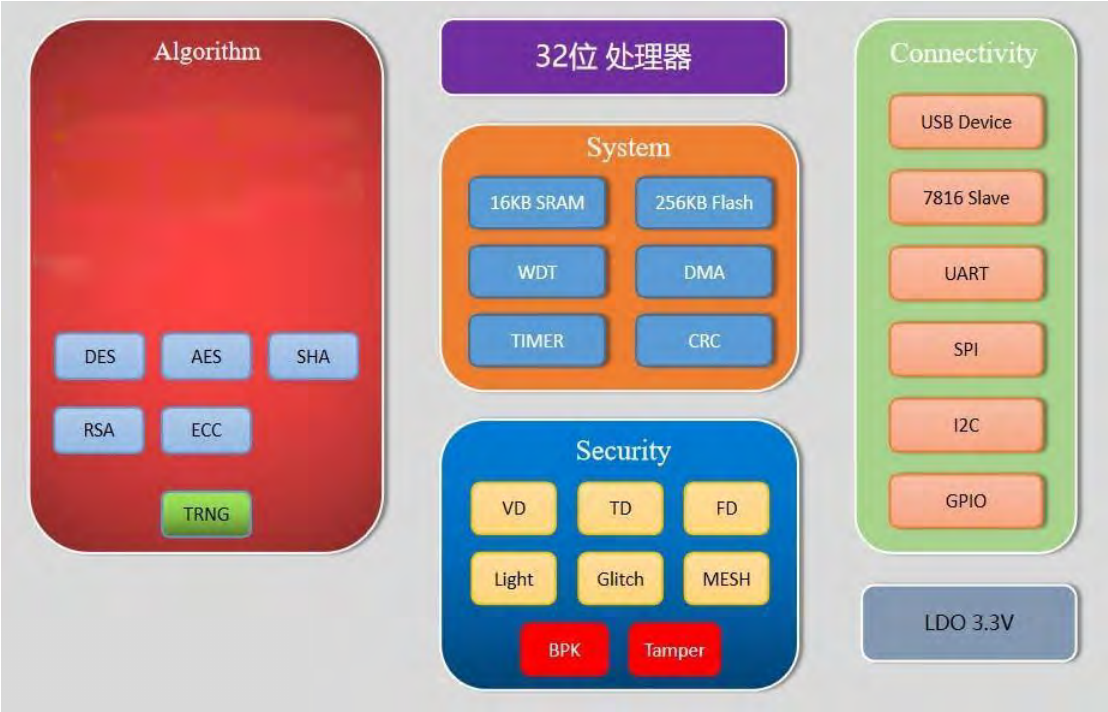


Figure 1 Block Diagram of MH1721

2 Characteristics

2.1 Electrical characteristics

Table 1 Ultimate Parameters

Parameters	Note	Range	Unit
VDD33	LDO output voltage	● VCC >= 3.3 ■ 3.2~3.3 ● VCC >= 2 and VCC <3.2 ■ 2.0~3	V
IddLdodrive	LDO drive current	70	mA
Iddpd	Shutdown current	--	nA
Tamb	Operating temperature	-40~+85	℃
Tstg	Storage temperature	-40~+125	℃
Ground	Ground	-0.3~0.3	V
Voh	Digital output high level	VDD -0.3 ~ VDD+0.3	V
Vol	Digital output low level	<0.4	V
Ioh	Source current	4/8	mA
Iol	Sink current	4/8	mA
Vih	Digital input high level	≥0.7×VDD	V
ViL	Digital input low level	≤0.3×VDD	V

Table 2 Electrical Characteristics

Parameters	Condition(-40℃ to +85℃)	Value		Unit
		Minimum	Maximum	
VCC		1.9	5.5	V
VBAT33		1.8	3.6	V
Vol	VDD=3.3V	-	0.4	V
Voh	VDD=3.3V	VDD – 0.3	-	V
VIH	VDD=3.3V	0.7×VDD	-	V
VIL	VDD=3.3V	-	0.3×VDD	V

Table 3 Safety-related Characteristics

Sensor	Note	Range	Unit
Temperature sensor	High temperature detection range	100±15	℃
	Low temperature detection range	-30 ~ -40	℃
Voltage sensor	High voltage detection range of main power voltage	5.8±0.1	V
	Low voltage detection range of main power voltage	1.8±0.1	V
	High voltage detection range of VBAT voltage	5.8±0.1	V
	Low voltage detection range of VBAT voltage	1.8±0.1	V

Table 4 List of Power Consumption

Operating Mode	Note	Power consumption	Unit
RUN	● All peripherals are turned on ■ @80MHz ■ @40MHz	9 6	mA
	● All peripherals are turned off ■ @80MHz ■ @40MHz	4.7 2.7	
CPU Sleep	All peripherals are turned off @80MHz	1.2	mA
Deep Sleep	Support IO high/low level, BPU attack wake-up	80	uA
Power Down	Support IO low level wake-up	1.6	uA
VBAT33	QFN16_SE package	1.6	uA

2.2 Definition of pins

2.2.1 QFN16_SE

Table 5 Definitions of MH1721 QFN16_SE 3mm×3mm Packaging Pins

PIN No.	PIN name	Remark
1	GPIO1	Boot download UART TX
2	GPIO2	
3	GPIO3	
4	DP	USB DP
5	DN	USB DN
6	GPIO7	Boot download SPI MISO
7	VCC	Chip power supply
8	VBAT33	Button battery powered
9	EXTS3	External Tamper3
10	EXTS2	External Tamper2
11	EXTS1	External Tamper1
12	EXTS0	External Tamper0
13	GPIO6	Boot download SPI MOSI
14	GPIO5	Boot download SPI CS
15	GPIO4	Boot download SPI CLK
16	GPIO0	Boot download UART RX

2.2.2 QFN16_UK

Table 6 Definitions of MH1721 QFN16_UK 3mm×3mm Packaging Pins

PIN No.	PIN name	Remark
1	GPIO2	
2	GPIO3	
3	DP	USB DP
4	DN	USB DN
5	GPIO7	Boot download SPI MISO
6	VDD33_OUT	3.3V LDO output
7	VCC	Chip power supply
8	NC	
9	NC	
10	GPIO4	Boot download SPI CLK
11	GPIO5	Boot download SPI CS
12	GPIO6	Boot download SPI MOSI
13	RSTN	Reset pin
14	**VSS**	Ground
15	GPIO0	Boot download UART RX
16	GPIO1	Boot download UART TX

2.2.3 DFN10

Table 7 Definitions of MH1721 DFN10 3mm×3mm Packaging Pins

PIN No.	PIN name	Remark
1	**VSS**	Ground
2	GPIO4	Serial Data Line (SDA)
3	NC	
4	NC	
5	NC	
6	GPIO0	Boot download UART RX
7	GPIO1	Boot download UART TX
8	GPIO3	Serial Clock Line (SCL)
9	RSTN	Reset pin
10	VCC	Chip power supply

2.2.4 SOP8

Table 8 Definitions of MH1721 SOP8 Packaging Pins

PIN No.	PIN name	Remark
1	GPIO0	Boot download UART RX
2	GPIO1	Boot download UART TX
3	GPIO6	Boot download SPI MOSI
4	**GND**	Ground
5	GPIO4	Boot download SPI CLK
6	GPIO5	Boot download SPI CS
7	GPIO7	Boot download SPI MISO
8	**VCC**	Chip power supply

2.3 Information on package

2.3.1 QFN16

标注 \ 尺寸	最小	标准	最大	标注 \ 尺寸	最小	标准	最大
A	0.70	0.75	0.80	D1	1.60	1.70	1.80
A1	0.00	—	0.05	E1	1.60	1.70	1.80
A3		0.203REF		e		0.50TYP	
b	0.20	0.25	0.30	K	0.20	-	-
D	2.90	3.00	3.10	L	0.30	0.40	0.50
E	2.90	3.00	3.10				

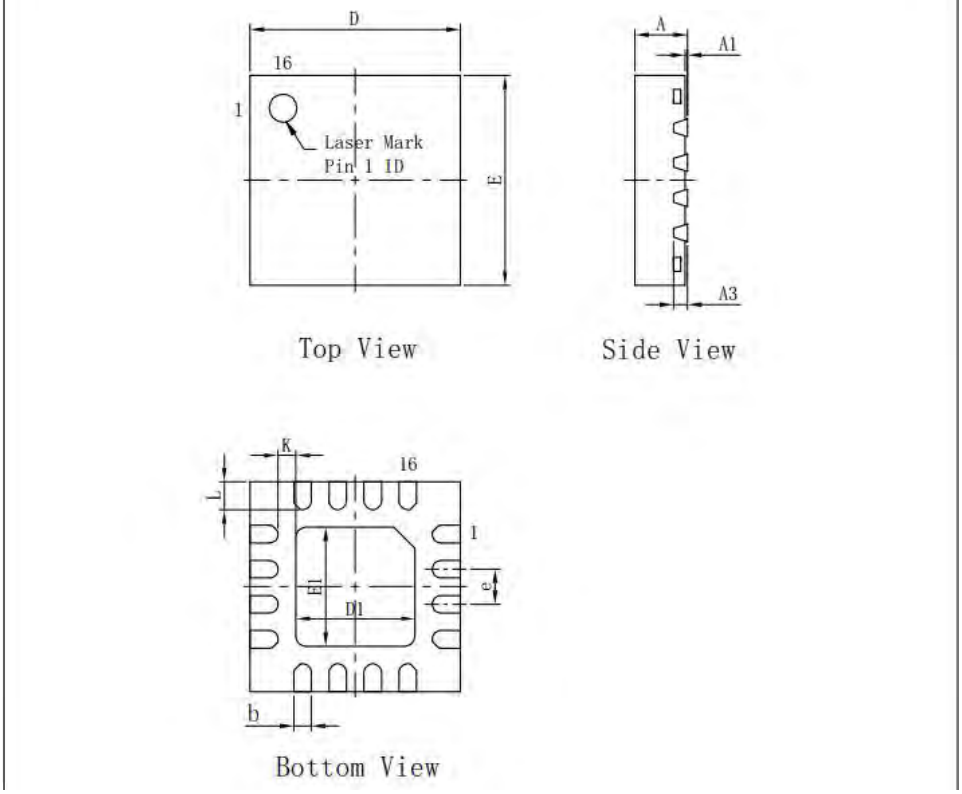


Figure 2 MH1721 QFN16 3mm×3mm package dimension

标注 \ 尺寸	最小(mm)	标准(mm)	最大(mm)	标注 \ 尺寸	最小(mm)	标准(mm)	最大(mm)
A	0.70	0.75	0.80	E	2.90	3.00	3.10
A1	–	–	0.05	D2	1.60	1.70	1.80
A3		0.203 REF		E2	2.30	2.40	2.50
b	0.18	0.23	0.28	e		0.50 TYP	
D	2.90	3.00	3.10	L	0.35	0.40	0.45

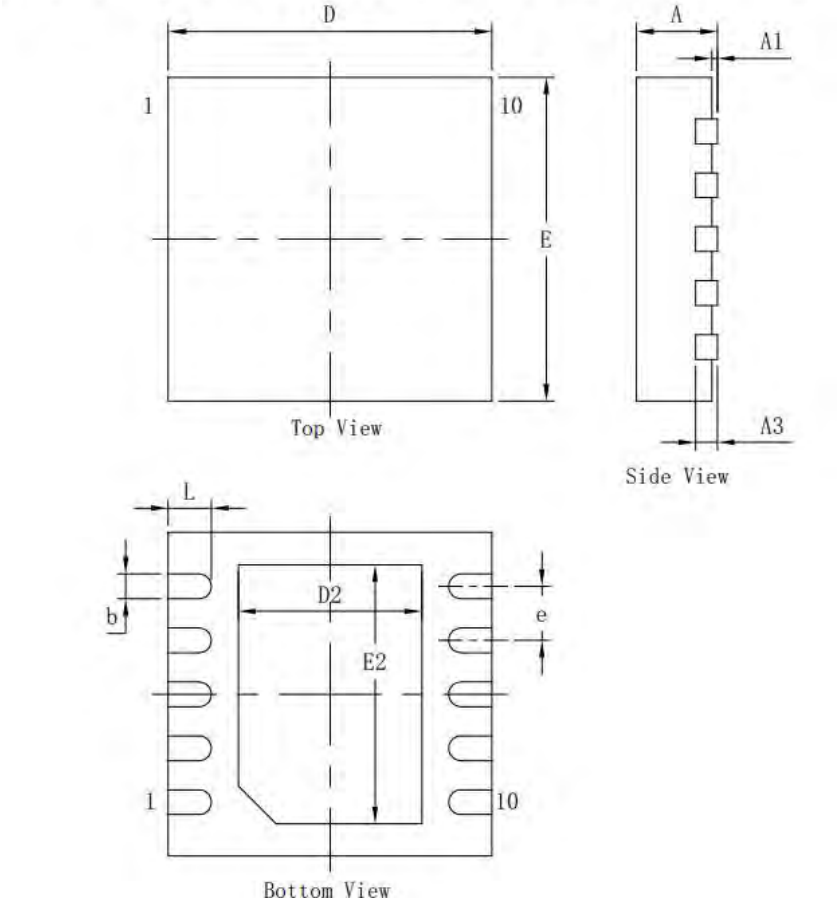
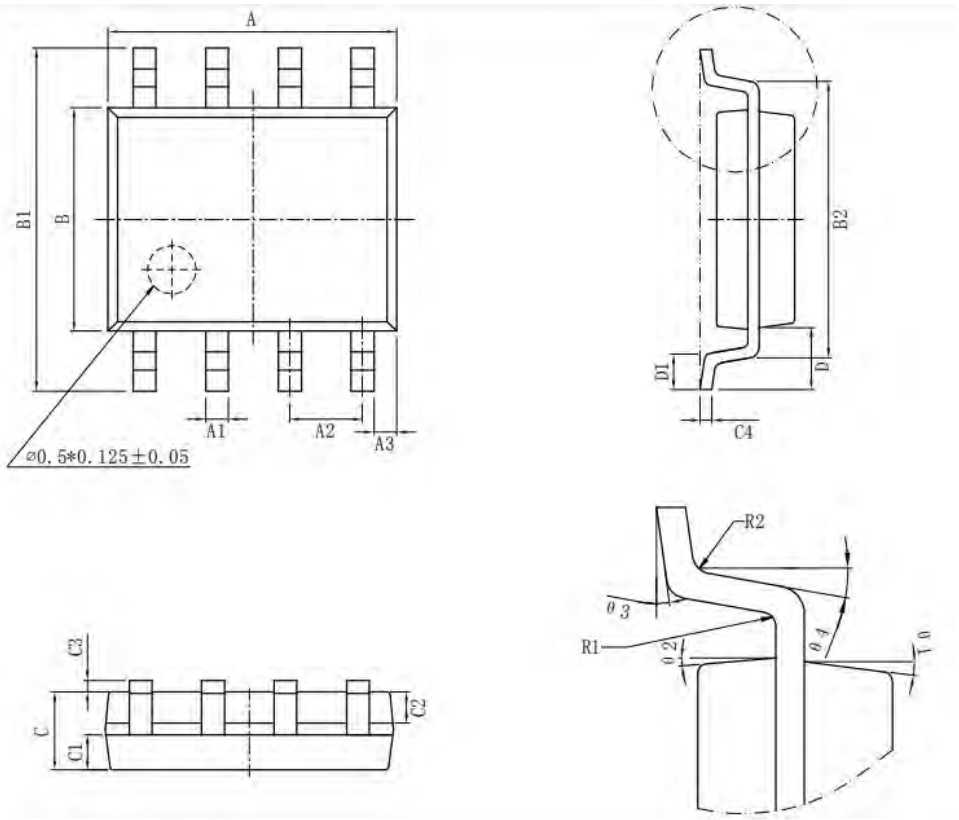


Figure 3 MH1721 DFN10 3mm×3mm package dimension

2.3.2 SOP8



标注 \ 尺寸	最小(mm)	最大(mm)	标注 \ 尺寸	最小(mm)	最大(mm)
A	4.80	5.00	C3	0.05	0.20
A1	0.356	0.456	C4	0.203	0.233
A2	1.27TYP		D	1.05TYP	
A3	0.345TYP		D1	0.40	0.80
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
B2	5.00TYP		θ1	17° TYP4	
C	1.30	1.60	θ2	13° TYP4	
C1	0.55	0.65	θ3	0° ~ 8°	
C2	0.55	0.65	θ4	4° ~ 12°	

Figure 4 MH1721 SOP8 150mil package dimension

2.4 Ordering Information on part numbers

Table 9 MH1721 part numbers

Ordering Information (Part Numbers)	SRAM	Flash	Package
MH1721S14CE00	16KB	256KB	SOP8
MH1721DE4CE00	16KB	256KB	DFN10
MH1721QF4CES0	16KB	256KB	QFN16_SE

3 Details of Functional Modules

3.1 Description of peripherals

3.1.1 SPI

MH1721 provides 1 SPI master/slave, which can support communication with multiple slave devices when used as the master device interface.

Characteristics of SPI peripherals:

- Operation of Master mode and Slave mode at independent address
- Master mode supports full duplex, simplex receiving, simplex transmitting mode
- Multiple Master conflict detections
- Receive and transmit FIFO independently at the depth of 64
- DMA interface

The common Motorola SPI communication protocol supports four communication modes, so as to achieve full duplex communication. The default mode 0 is used to power on the system.

The four communication formats as specified in SPI protocol are described as follows:

- Mode 0: Clock polarity (CPOL) = 0, clock phase (CPHA) = 0. In this mode, the idle state of the serial synchronous clock is low. MH1721 samples data on the clock's first rising edge. This mode is default mode.
- Mode 1: Clock polarity (CPOL) = 0, clock phase (CPHA) = 1. In this mode, the idle state of the serial synchronous clock is low. MH1721 samples data on the clock's second falling edge;
- Mode 2: Clock polarity (CPOL) = 1, clock phase (CPHA) = 0. In this mode, the idle state of the serial synchronous clock is high. MH1721 samples on the clock’s first falling edge.
- Mode 3: Clock polarity (CPOL) = 1, clock phase (CPHA) = 1. In this mode, the idle state of the serial synchronous clock is high. MH1721 samples data on the clock’s second rising edge.

Note: In order to keep the normal operation of the MH1721 SPI, ensure that the CSN signal line is kept at a high level during mode switching. At the same time, when the master thinks that the slave has an error during the communication process, it can restore the slave to normal by pulling CSN high.

SPI interfaces are described as follows:

- SCK: The clock input pin of SPI; when the communication rate of 200K is adopted, the delay of 20us is needed between the bytes as a minimum;
- CSN: MH1721 selection signal of SPI, which is the input pin of MH1721, with low

efficiency;

- MOSI: The data input pin of SPI;
- MISO: The data output pin of SPI.

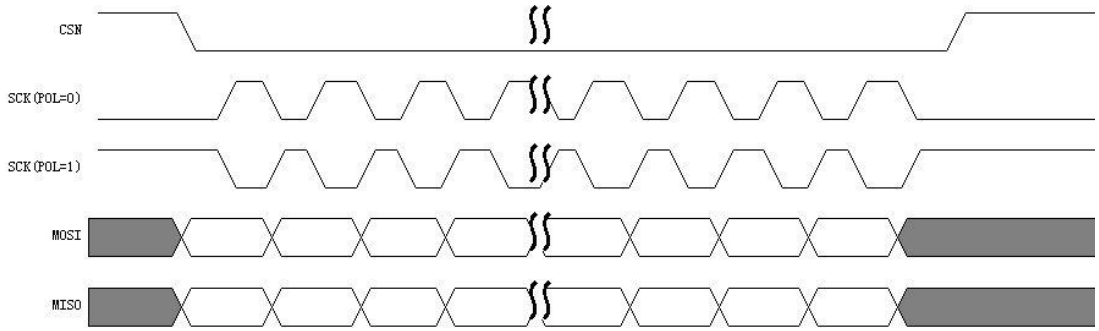


Figure 5 SPI Time Sequence 1 (CPHA=0)

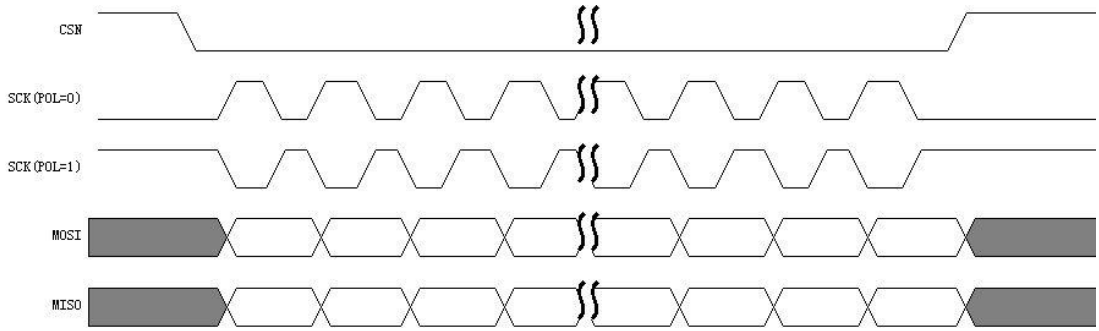


Figure 6 SPI Time Sequence 2(CPHA=1)

3.1.2 UART

MH1721 has one full-duplex UART serial communication interface, which supports 4-wire mode.

Characteristics of UART peripherals:

- Receive and transmit FIFO independently at the depth of 16 bytes;
- Control of FIFO enabling
- Setting of data bits, supporting 5-8bit
- Forced output of 9 check bits
- Frame error, check error, break interrupt detection
- DMA receiving

UART peripherals support independent receiving and transmitting of FIFO, and FIFO function can be configured for use by enabling bits.

The receiving and transmitting of FIFO by UART supports the full interrupt in receiving FIFO and the empty interrupt in transmitting FIFO respectively, and the trigger values

thereof are configurable. The interrupt source in transmitting FIFO shares the same interrupt source with the transmitter holding register empty (THRE) in the non-FIFO mode, which is set by the software.

3.1.3 USB

USB1.1Device, support full speed mode

USB peripherals support USB suspend/resume operation, which can stop the device clock for low power consumption

- Compliance with the technical specifications of USB1.1 full-speed devices
- Support 4 bidirectional endpoints (including control endpoint)
- A total of 512 bytes of endpoint cache FIFO, of which 384 bytes can be configured to different endpoints as needed
- All endpoints share receive FIFO, optional share transmit FIFO

3.1.4 Sensor

MH1721 has built-in multiple environmental safety detection circuits. include:

- Clock frequency detection
- High and low temperature attack detection
- High and low voltage attack detection
- Light detection
- Active shielding
- Voltage glitch detection

3.1.5 GPIO

MH1721 supports up to 8 GPIOs, and each IO multiplexes pins with peripherals. Each GPIO can be configured as input, output, and interrupt mode; when GPIO is configured as output, each IO output value can be configured separately. IO supports strong push-pull/open-drain output modes.

3.1.6 DMA

Direct memory access (DMA) is used to provide high-speed data transmission between peripherals and memory or between memory and memory. Data can be moved quickly through DMA without CPU intervention, so as to free up CPU resources for other operations.

The DMA controller has eight channels, each of which is specially used to manage the requests for access from memory to memory, from memory to peripheral, and from peripheral to memory. The setting of independent priority is assigned to each channel.

The main characteristics include:

- 2 independent configurable channels

- 2 independent hardware DMA requests (DMA hard handshake interface), each channel also supports software departure (DMA soft handshake interface)
- Support multi-width data transmission
- Each channel has its own interrupt signal and flag
- Support the transmission from memory to memory, from memory to peripheral, and from peripheral to memory

FOR MORE INFORMATION

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