MEGAHUNT

COMW5
Brief Introduction

TCP/IP embedded Ethernet controller

Version: 1.0
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Megahunt Tehnologies Inc.

History of Revision

Date	Version	Description	Author
2014-11-24	1.00	Completed the first draft	MEGAHUNT

COMW5

The COMW5 chip is a Hardwired TCP/IP embedded Ethernet controller that provides easier Internet connection to embedded systems. COMW5 enables users to have the Internet connectivity in their applications just by using the single chip in which TCP/IP stack, 10/100 Ethernet MAC and PHY embedded.

Megahunt's Hardwired TCP/IP is the market-proven technology that supports TCP, UDP, IPv4, ICMP, ARP, IGMP, and PPPoE protocols. COMW5 embeds the 32Kbyte internal memory buffer for the Ethernet packet processing. If you use COMW5, you can implement the Ethernet application just by adding the simple socket program. It's faster and easier way rather than using any other Embedded Ethernet solution. Users can use 8 independent hardware sockets simultaneously.

SPI (Serial Peripheral Interface) is provided for easy integration with the external MCU. The COMW5's SPI supports 80 MHz speed and new efficient SPI protocol for the high speed network communication. In order to reduce power consumption of the system, COMW5 provides WOL (Wake on LAN) and power down mode.

Features

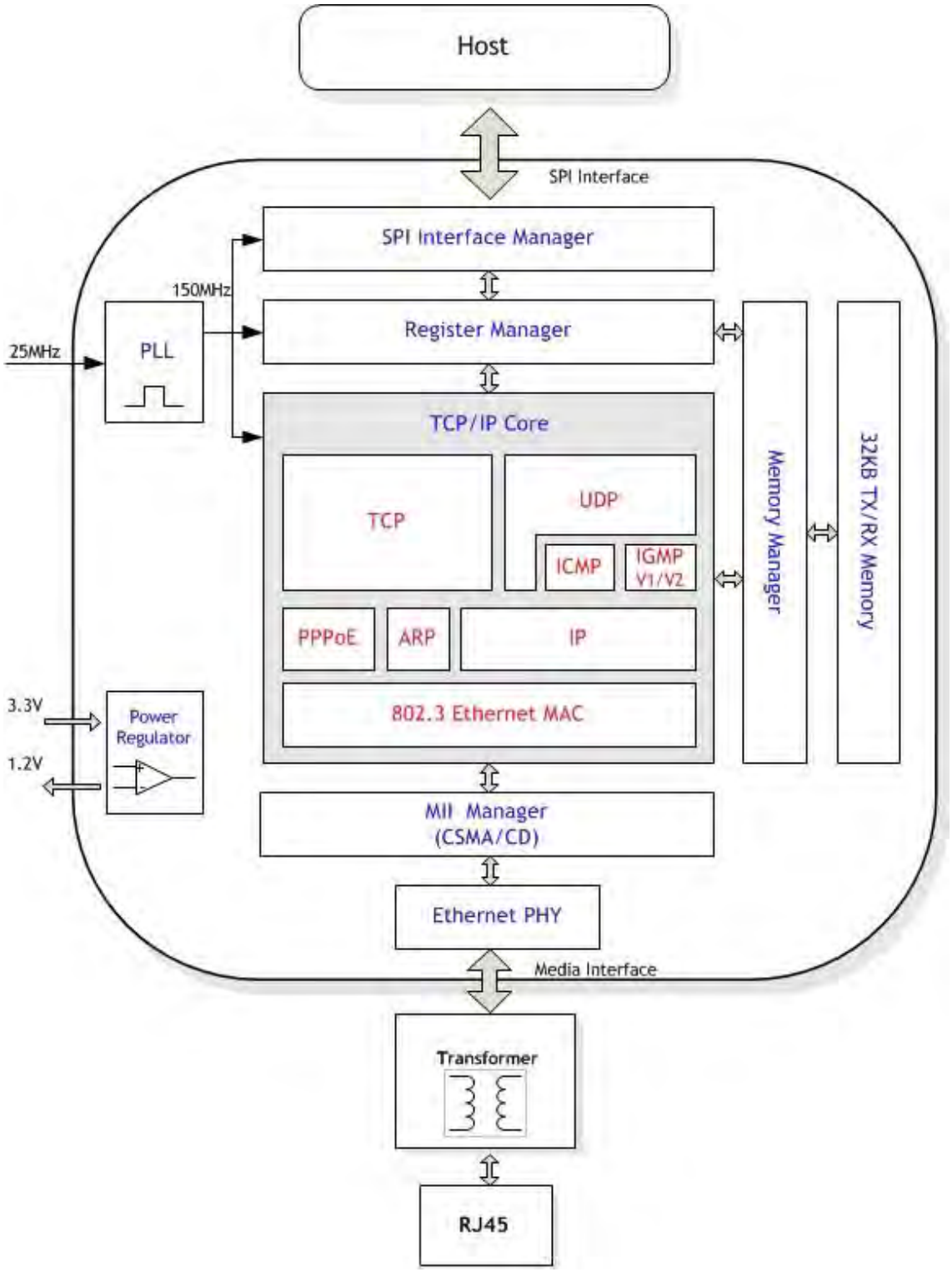
- Supports Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMP, PPPoE
- Supports 8 independent sockets simultaneously
- Supports Power down mode
- Supports Wake on LAN over UDP
- Supports High Speed Serial Peripheral Interface(SPI MODE 0, 3)
- Internal 32Kbytes Memory for TX/RX Buffers
- 10BaseT/100BaseTX Ethernet PHY embedded
- Supports Auto Negotiation (Full and half duplex, 10 and 100-based)
- Not supports IP Fragmentation
- 3.3V operation with 5V I/O signal tolerance
- LED outputs (Full/Half duplex, Link, Speed, Active)
- 48 Pin LQFP Lead-Free Package (7x7mm, 0.5mm pitch)

Target Applications

COMW5 is suitable for the following embedded applications:

- Home Network Devices: Set-Top Boxes, PVRs, Digital Media Adapters
- Serial-to-Ethernet: Access Controls, LED displays, Wireless AP relays, etc.
- Parallel-to-Ethernet: POS / Mini Printers, Copiers
- USB-to-Ethernet: Storage Devices, Network Printers
- GPIO-to-Ethernet: Home Network Sensors
- Security Systems: DVRs, Network Cameras, Kiosks
- Factory and Building Automations
- Medical Monitoring Equipment
- Embedded Servers

Block Diagram



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1 Pin Assignment

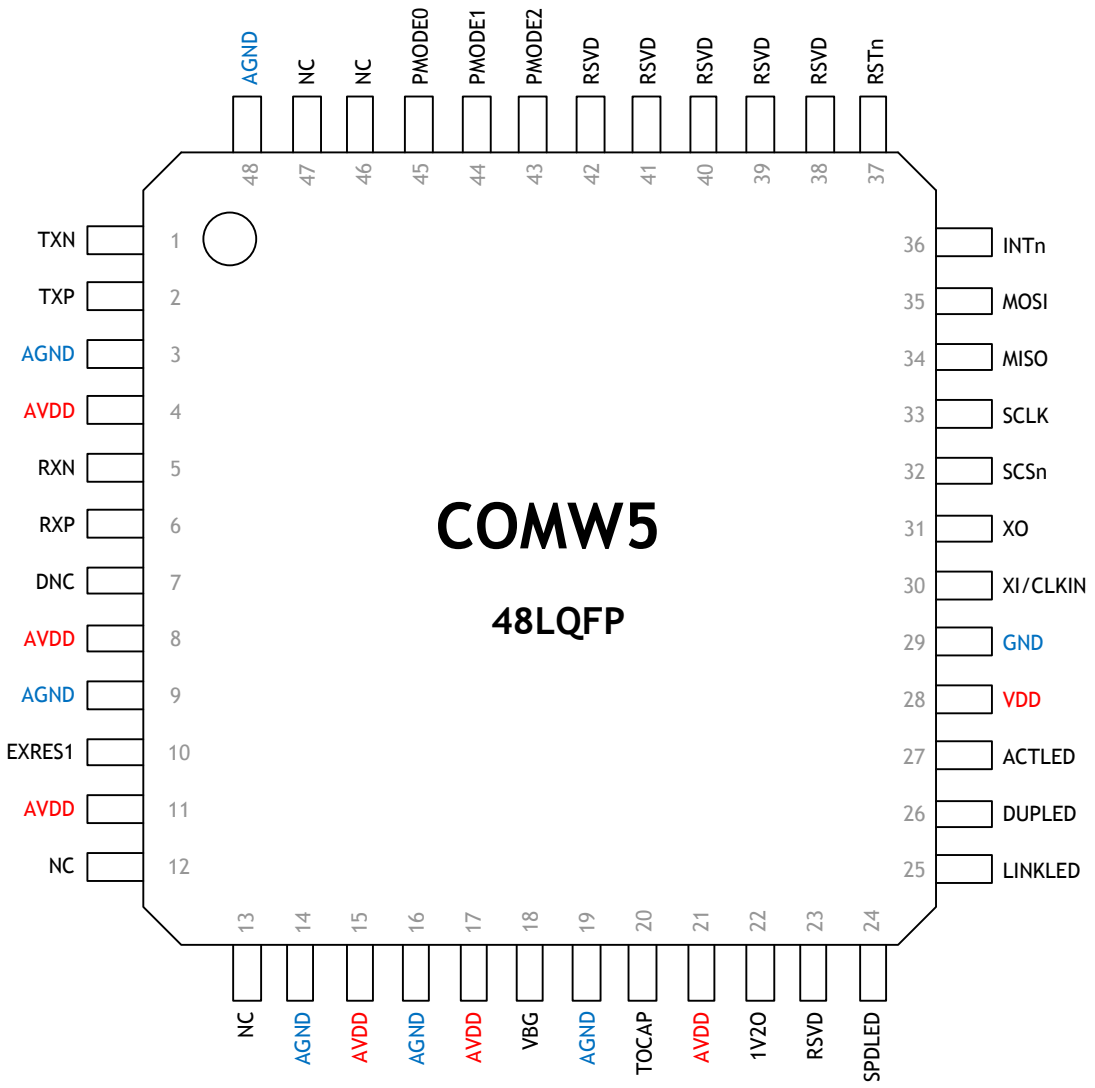


Figure 1. COMW5 Pin Layout

1.1 Pin Descriptions

Table 1. Pin Type Notation

Type	Description
I	Input
O	Output
I/O	Input / Output
A	Analog
PWR	3.3V power
GND	Ground

Table 2. COMW5 Pin Description

Pin No	Symbol	Internal Bias[1]	Type	Description
1	TXN	-	AO	**TXP/TXN Signal Pair**
2	TXP	-	AO	The differential data is transmitted to the media on the TXP/TXN signal pair.
3	AGND	-	GND	**Analog ground**
4	AVDD	-	PWR	**Analog 3.3V power**
5	RXN	-	AI	**RXP/RXN Signal Pair**
6	RXP	-	AI	The differential data from the media is received on the RXP/RXN signal pair.
7	DNC	-	AI/O	**Do Not Connect Pin**
8	AVDD	-	PWR	**Analog 3.3V power**
9	AGND	-	GND	**Analog ground**
10	EXRES1	-	AI/O	**External Reference Resistor** It should be connected to an external resistor (12.4KΩ, 1%) needed for biasing of internal analog circuits. Refer to the 'External reference resistor' (Figure.2) for details.
11	AVDD	-	PWR	**Analog 3.3V power**
12	-		-	**NC**
13	-		-	**NC**
14	AGND	-	GND	**Analog ground**
15	AVDD	-	PWR	**Analog 3.3V power**
16	AGND	-	GND	**Analog ground**
17	AVDD	-	PWR	**Analog 3.3V power**
18	VBG	-	AO	**Band Gap Output Voltage** This pin will be measured as 1.2V at 25℃. It must be left floating.
19	AGND	-	GND	**Analog ground**
20	TOCAP	-	AO	**External Reference Capacitor** This pin must be connected to a 4.7uF capacitor. The trace length to capacitor should be short to stabilize the internal signals.
21	AVDD	-	PWR	**Analog 3.3V power**
22	1V2O	-	AO	**1.2V Regulator output voltage**

[1] Internal Bias after hardware reset

				This pin must be connected to a 10nF capacitor. This is the output voltage of the internal regulator.
23	RSVD	Pull-down	I	It must be tied to GND.
24	SPDLED	-	O	**Speed LED** This shows the Speed status of the connected link. Low: 100Mbps High: 10Mbps
25	LINKLED	-	O	**Link LED** This shows the Link status. Low: Link is established High: Link is not established
26	DUPLED	-	O	**Duplex LED** This shows the Duplex status for the connected link. Low: Full-duplex mode High: Half-duplex mode
27	ACTLED	-	O	**Active LED** This shows that there is Carrier sense (CRS) from the active Physical Medium Sub-layer (PMD) during TX or RX activity. Low: Carrier sense from the active PMD High: No carrier sense
28	VDD	-	PWR	**Digital 3.3V Power**
29	GND	-	GND	**Digital Ground**
30	XI/CLKIN	-	AI	**Crystal input / External Clock input** External 25MHz Crystal Input. This pin can also be connected to single-ended TTL oscillator (CLKIN). 3.3V clock should be applied for the External Clock input. If this method is implemented, XO should be left unconnected. Refer to the 'Crystal reference schematic' (Figure.3) for details.
31	XO	-	AO	**Crystal output** External 25MHz Crystal Output Note: Float this pin if using an external clock being driven through XI/CLKIN
32	SCSn	Pull-up	I	**Chip Select for SPI bus** This pin can be asserted low to select COMW5 in SPI interface.

<table>
<tr><td></td><td></td><td></td><td></td><td>Low: selected
High: deselected</td></tr>
<tr><td>33</td><td>SCLK</td><td>-</td><td>I</td><td>SPI clock input
This pin is used to receive SPI Clock from SPI master.</td></tr>
<tr><td>34</td><td>MISO</td><td>-</td><td>O</td><td>SPI master input slave(COMW5) output
When SCSn is Low, this pin outputs SPI data.
When SCSn is High, this pin becomes High Impedance (logically disconnected).</td></tr>
<tr><td>35</td><td>MOSI</td><td>-</td><td>I</td><td>SPI master output slave(COMW5) input</td></tr>
<tr><td>36</td><td>INTn</td><td>-</td><td>O</td><td>Interrupt output
(Active low)
Low: Interrupt asserted from COMW5
High: No interrupt</td></tr>
<tr><td>37</td><td>RSTn</td><td>Pull-up</td><td>I</td><td>Reset
(Active low)
RESET should be held low at least 500 us for COMW5 reset.</td></tr>
<tr><td>38</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>39</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>40</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>41</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>42</td><td>RSVD</td><td>Pull-down</td><td>I</td><td>NC</td></tr>
<tr><td>43</td><td>PMODE2</td><td>Pull-up</td><td>I</td><td rowspan="3">PHY Operation mode select pins
These pins determine the network mode. Refer to the below table for details.
<table>
<tr><th colspan="3">PMODE [2:0]</th><th rowspan="2">Description</th></tr>
<tr><th>2</th><th>1</th><th>0</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>10BT Half-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>10BT Full-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>100BT Half-duplex, Auto-negotiation disabled</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>100BT Full-duplex, Auto-negotiation disabled</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>100BT Half-duplex, Auto-negotiation enabled</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Not used</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Not used</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>All capable, Auto-negotiation enabled</td></tr>
</table></td></tr>
<tr><td>44</td><td>PMODE1</td><td>Pull-up</td><td>I</td></tr>
<tr><td>45</td><td>PMODE0</td><td>Pull-up</td><td>I</td></tr>
<tr><td>46</td><td>-</td><td>-</td><td>-</td><td>NC</td></tr>
<tr><td>47</td><td>-</td><td>-</td><td>-</td><td>NC</td></tr>
<tr><td>48</td><td>AGND</td><td>-</td><td>GND</td><td>Analog ground</td></tr>
</table>

2 HOST Interface

COMW5 provides SPI (Serial Peripheral Interface) Bus Interface with 4 signals (SCSn, SCLK, MOSI, MISO) for external HOST interface, and operates as a SPI Slave.

The COMW5 SPI can be connected to MCU as shown in Figure 4 and Figure 5 according to its operation mode (Variable Length Data / Fixed Length Data Mode) which will be explained in Chapter 2.3 and Chapter 2.4.

In Figure 4, SPI Bus can be shared with other SPI Devices. Since the SPI Bus is dedicated to COMW5, SPI Bus cannot be shared with other SPI Devices. It is shown in Figure 5.

At the Variable Length Data mode (as shown in Figure 4), it is possible to share the SPI Bus with other SPI devices. However, at the Fixed Length Data mode (as shown in Figure 5), the SPI Bus is dedicated to COMW5 and can't be shared with other devices.

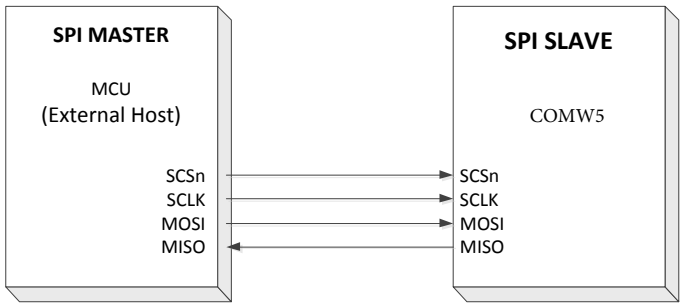


Figure 2. Variable Length Data Mode (SCSn controlled by the host)

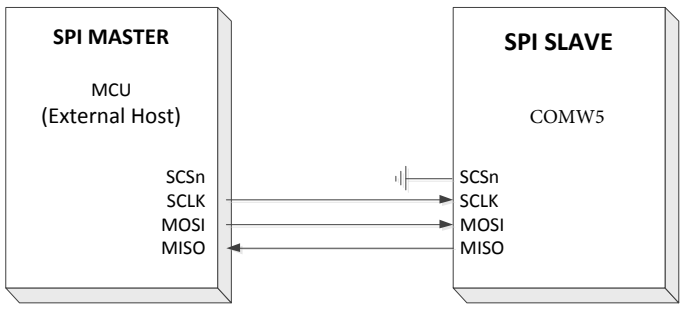
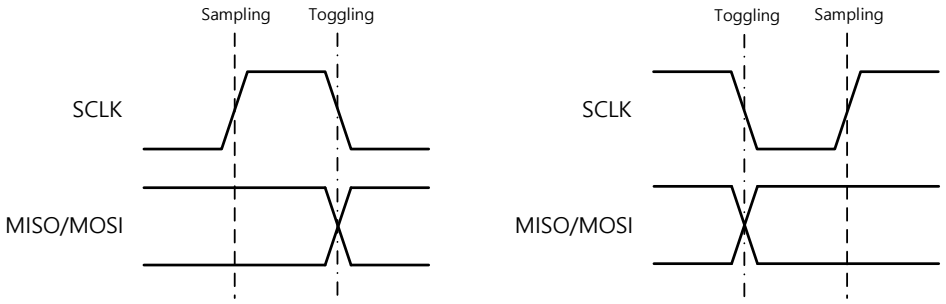


Figure 3. Fixed Length Data Mode (SCSn is always connected by Ground)

The SPI protocol defines four modes for its operation (Mode 0, 1, 2, 3).Each mode differs according to the SCLK polarity and phase. The only difference between SPI Mode 0 and SPI Mode 3 is the polarity of the SCLK signal at the inactive state.

With SPI Mode 0 and 3, data is always latched in on the rising edge of SCLK and always output on the falling edge of SCLK.

The COMW5 supports SPI Mode 0 and Mode 3. Both MOSI and MISO signals use transfer sequence from Most Significant Bit (MSB) to Least Significant Bit (LSB) when MOSI signal transmits and MISO signal receives. MOSI & MISO signals always transmit or receive in sequence from the Most Significant Bit (MSB) to Least Significant Bit (LSB).



Mode 0 : SCLK idle level low

Mode 3 : SCLK idle level high

Figure 4. SPI Mode 0 & 3

3 Register and Memory Organization

COMW5 has one Common Register Block, eight Socket Register Blocks, and TX/ RX Buffer Blocks allocated to each Socket. Each block is selected by the BSB[4:0] (Block Select Bit) of SPI Frame. Figure 20 shows the selected block by the BSB[4:0] and the available offset address range of Socket TX/RX Buffer Blocks. Each Socket's TX Buffer Block exists in one 16KB TX memory physically and is initially allocated with 2KB. Also, Each Socket's RX Buffer Block exists in one 16KB RX Memory physically and is initially allocated with 2KB.

Regardless of the allocated size of each Socket TX/RX Buffer, it can be accessible within the 16 bits offset address range (From 0x0000 to 0xFFFF).

Refer to 'Chapter 3.3' for more information about 16KB TX/RX Memory organization and access method.

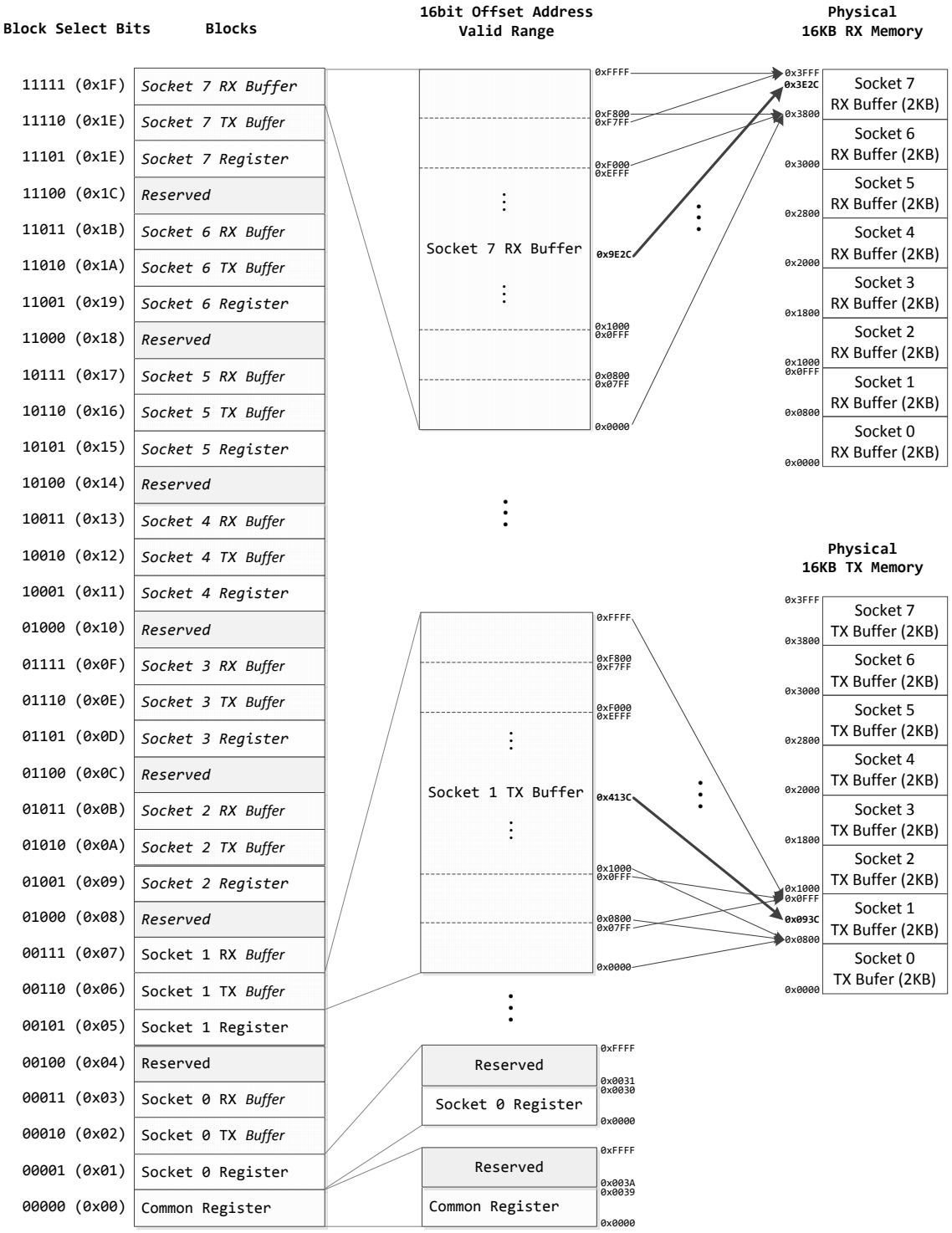


Figure 5. Register & Memory Organization

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DD}	DC Supply voltage	-0.5 to 4.6	V
V_{IN}	DC input voltage	-0.5 to 6	V
V_{OUT}	DC output voltage	-0.5 to 4.6	V
I_{IN}	DC input current	±5	mA
T_{OP}	Operating temperature	-40 to +85	°C
T_{STG}	Storage temperature	-65 to +150	°C

***COMMENT**: Stressing the device beyond the 'Absolute Maximum Ratings' may cause permanent damage.

4.2 Absolute Maximum Ratings (Electrical Sensitivity)

Electrostatic discharge (ESD)

Symbol	Parameter	Test Condition	Class	Maximum value(1)	Unit
VESD(HBM)	Electrostatic discharge voltage (human body model)	TA = +25 °C conforming to MIL-STD 883F Method 3015.7	2	2000	V
VESD(MM)	Electrostatic discharge voltage (man machine model)	TA = +25 °C conforming to JEDEC EIA/JESD22 A115-A	B	200	V
VESD(CDM)	Electrostatic discharge voltage (charge device model)	TA = +25 °C conforming to JEDEC JESD22 C101-C	III	500	V

Static latchup

Symbol	Parameter	Test Condition	Class	Maximum value(1)	Unit
LU	Static latch-up class	TA = +25 °C conforming to JESD78A	I	≥ ±200	mA

4.3 DC Characteristics

(Test Condition: Ta = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Supply voltage	Apply VDD, AVDD	2.97	3.3	3.63	V
V_{IH}	High level input voltage		2.0		5.5	V
V_{IL}	Low level input voltage		- 0.3		0.8	V
V_T	Threshold point	All inputs except XI	1.30	1.41	1.53	V
V_{T+}	Schmitt trig Low to High Threshold point	All inputs except XI	1.53	1.64	1.73	V
V_{T-}	Schmitt trig High to Low Threshold point	All inputs except XI	0.95	1.02	1.09	V
T_J	Junction temperature		0	25	125	°C
I_L	Input Leakage Current				±1	μA
R_{PU}	Pull-up Resistor	SCSn, RSTn, PMODE[2:0]	62	77	112	Kohm
R_{PD}	Pull-down Resistor	RSVD(Pin 23, Pin 38 ~ Pin 42)	48	85	174	Kohm
V_{OL}	Low level output voltage	IOL = 8mA, All outputs except XO			0.4	V
V_{OH}	High level output voltage	IOH = 8mA, All outputs except XO	2.4			V
I_{OL}	Low level output Current	VOL = 0.4V, All outputs except XO	8.6	13.9	18.9	mA
I_{OH}	High level output Current	VOH = 2.4V, All outputs except XO	12.5	26.9	47.1	mA
I_{DD1}	Supply Current (Normal operation mode)	VDD=3.3V, AVDD=3.3V, Ta = 25°C		132		mA
I_{DD2}	Supply Current (Power Down mode)	PHY Power Down mode, VDD=3.3V, AVDD=3.3V, Ta = 25°C		13		mA

4.4 Power Dissipation

(Test Condition: VDD=3.3V, AVDD=3.3V, Ta = 25°C)

Condition	Min	Typ	Max	Unit
100M Link	-	128	-	mA
10M Link	-	75	-	mA
Un-Link (Auto-negotiation mode)	-	65	-	mA
100M Transmitting	-	132	-	mA
10M Transmitting	-	79	-	mA
Power Down mode	-	13	-	mA

4.5 AC Characteristics

4.5.1 Reset Timing

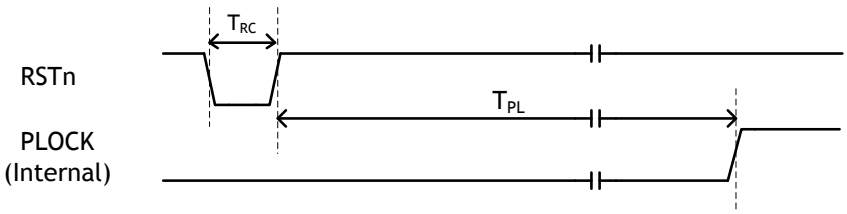


Figure 6. Reset Timing

Symbol	Description	Min	Max
T_{RC}	Reset Cycle Time	500 us	-
T_{PL}	RSTn to internal PLOCK (PLL Lock)	-	1 ms

4.5.2 Wake up Time

Voltage Regulator Wake up Time: **10us**

4.5.3 Crystal Characteristics

Parameter	Range
Frequency	25 MHz
Frequency Tolerance (at 25℃)	±30 ppm
Shunt Capacitance	7pF Max
Drive Level	59.12uW/MHz
Load Capacitance	18pF
Aging (at 25℃)	±3ppm / year Max

4.5.4 SPI Timing

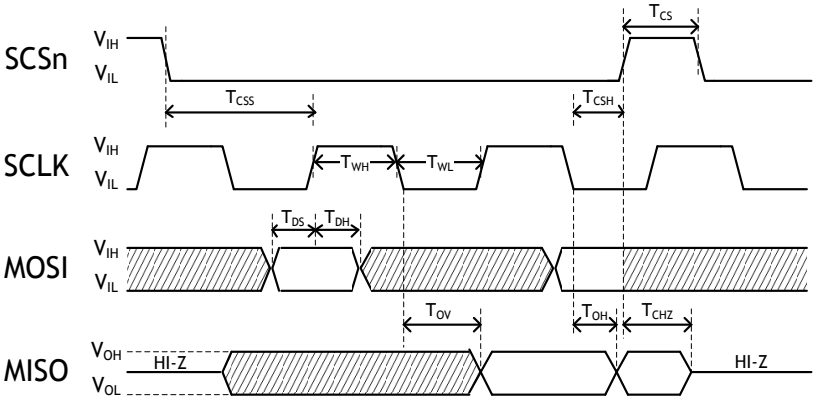


Figure 7. SPI Timing

Symbol	Description	Min	Max	Units
F_{SCK}	SCK Clock Frequency		80/33.3[4]	MHz
T_{WH}	SCK High Time	6		ns
T_{WL}	SCK Low Time	6		ns
T_{CS}	SCSn High Time	30		ns
T_{CSS}	SCSn Setup Time	5	-	ns
T_{CSH}	SCSn Hold Time	5		ns
T_{DS}	Data In Setup Time	3		ns
T_{DH}	Data In Hold Time	3		ns
T_{OV}	Output Valid Time		5	ns
T_{OH}	Output Hold Time	0		ns
T_{CHZ}	SCSn High to Output Hi-Z		2.1[5]	ns

[4] Theoretical Guaranteed Speed

Even though theoretical design speed is 80MHz, the signal in the high speed may be distorted because of the circuit crosstalk and the length of the signal line. The minimum guaranteed speed of the SCLK is 33.3 MHz which was tested and measured with the stable waveform.

Please refer to the SPI Application Note which shows the Megahunt test environment and results.

[5] 2.1ns is when pn loaded with 30pF. The time is shorter with lower capacitance.

4.5.5 Transformer Characteristics

Parameter	Transmit End	Receive End
Turn Ratio	1:1	1:1
Inductance	350 uH	350 uH

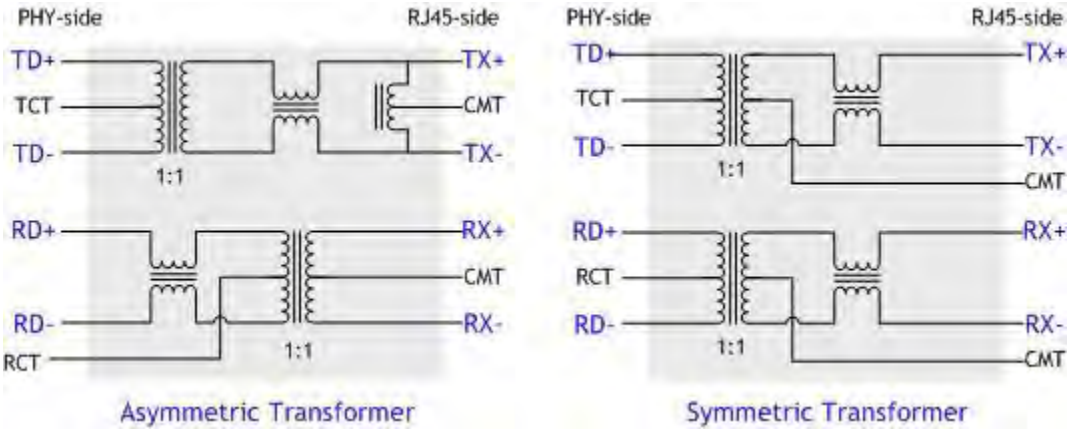


Figure 8. Transformer Type

4.5.6 MDIX

COMW5 does not support auto-MDIX feature.

Thus, user should use straight-through cables to connect to other switches or routers and crossover cables to connect to devices such as servers, workstations or another COMW5. However, user can use either type of cable to connect to other devices with auto-MDIX enabled, and the interface automatically corrects for any incorrect cabling.

5 IR Reflow Temperature Profile (Lead-Free)

Moisture Sensitivity Level : 3

Dry Pack Required: Yes

Average Ramp-Up Rate (Ts_{max} to Tp)	3° C/second max.
Preheat	
- Temperature Min (Ts_{min})	150 °C
- Temperature Max (Ts_{max})	200 °C
- Time (ts_{min} to ts_{max})	60-120 seconds
Time maintained above:	
- Temperature (TL)	217 °C
- Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)	265 + 0/-5°C
Time within 5 °C of actual Peak Temperature (tp)	30 seconds
Ramp-Down Rate	6 °C/second max.
Time 25 °C to Peak Temperature	8 minutes max.

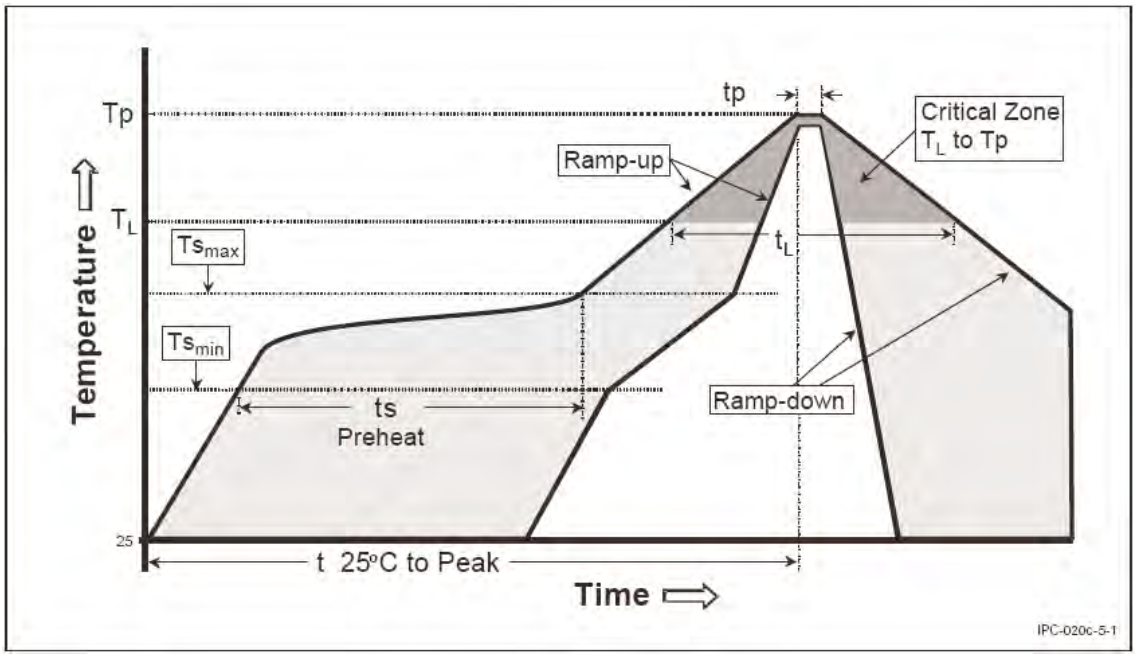
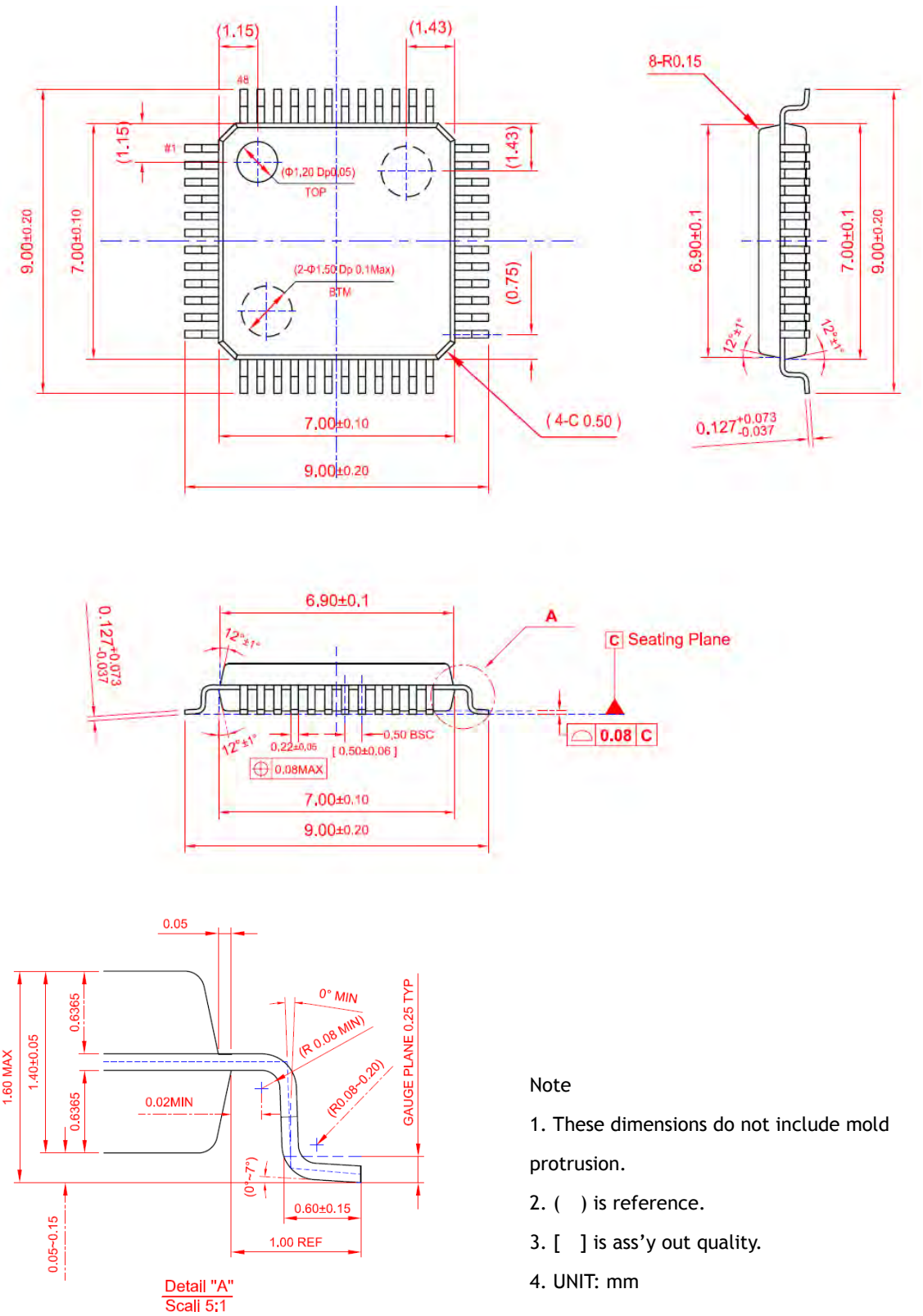


Figure 9. IR Reflow Temperature

6 Package Descriptions



Note

1. These dimensions do not include mold protrusion.
2. ( ) is reference.
3. [ ] is ass'y out quality.
4. UNIT: mm

Figure 10. Package Dimensions