MEGAHUNT

MH1706
Brief Introduction

Highly Integrated Secure SOC

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Megahunt Tehnologies Inc.

History of Revision

Date	Version	Description	Author
2020-05-03	1.00	Completed the first draft	MEGAHUNT
2020-06-17	1.10	Completed block diagram information	MEGAHUNT
2029-08-20	1.20	Added QFN20/SOP8/DFN8 pin definition	MEGAHUNT
2020-09-26	1.30	Added electrical parameters	MEGAHUNT
2021-2-18	1.50	Updated SOP8 pin definition	MEGAHUNT

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1 Overview

1.1 Description

The MH1706 has internal 32-bit RISC processor with up to 80MHz frequency. It is a low-cost, high-performance security device with USB 2.0 interface of high-speed and full-speed.

MH1706 has built-in symmetric algorithm encryption engine SCP (supports symmetric encryption algorithms such as DES/AES), asymmetric encryption co-processor ASCP (supports asymmetric algorithms such as RSA/ECC), and also supports Hash algorithms such as SHA160/224/256/384/512. In addition, MH1706 has built-in secure modules such as RNG/CRC. In order to improve safety and reliability, MH1706 provides various detection mechanisms such as voltage, frequency, temperature and light.

MH1706 supports MPU (memory protection unit), which can control the access authority to the memory.

MH1706 has built-in 32KB RAM, 384KB FLASH, and integrates various communication interfaces such as GPIO, USB, SPI, UART, I2C, etc. All peripheral driver software is compatible with the current mainstream security device software interfaces, which is in accordance with ARM CMSIS.

1.2 Main functions and characteristics

- 32-bit RISC processor
  - MPU memory protection unit
  - Maximum 80MHz main frequency(adjustable for 1,2,4,8,16 frequency division)
  - Support Privilege and unprivileged operating states
  - Low power consumption design
  - 1 controlled JTAG SW debugging port
- Memories
  - 32KB RAM
  - 384KB FLASH
    - Support page erasing and writing
    - More than 500,000 times of repeated erasing and rewriting, 10-year data retention
    - Page (512B) erasing time 50us
    - Writing 256 bytes time 400us
    - Full erasing time 15ms
- System control module (controls all peripheral module clocks and system-related configurations)
- Security encryption algorithm Co-processor

- ASCP Co-processor
  - ASCP clock can be configured for up to 80MHz
  - Support 512~2048 bits RSA operation, and support anti-SPA/DPA/FA/DFA function
  - Support 192/224/256/384/521 bits ECC operation, support anti-SPA/DPA/FA/DFA function
- DES/AES Co-processor
  - Support DES/3DES ECB/CBC mode operation
  - 3DES algorithm supports 2-KEY method
  - Support anti-SPA/DPA/FA/DFA function

- 2 UART interfaces (both support 4-wire)
- 2 SPI interfaces (one interface can be configured as master or slave, another one interface supports master only)
- 1 I2C interface
- 4 32-bit TIMER(with PWM function)
- Integrated internal watchdog
- 1 random number generator including true/pseudo-random number generation
- 1 DMA controller (supports 2-channel DMA transfer)
- 1 CRC module
- Support up to 24 GPIOs
- Internal environment monitoring Sensor (high and low voltage, high and low temperature, MESH, clock, light and voltage glitch detection)
- Support RTC
- 1 USB2.0 Device interface, support high-speed and full-speed
- Integrated USB charging management module, supporting the maximum charging current of 100mA
- Integrated LDO that can output 150mA drive capability
- Integrated the power-on/off function

1.3 Applications

Bank security token devices, security encryption modules, CA(Certification Authority) devices.

1.4 Package Types

- QFN32
- QFN20
- SOP8
- DFN8

1.5 Description of structure

MH1706 has internal 32-bit RISC processor, 32KB RAM, system control module, security encryption module, TRNG(true random number generator), one DMA controller, 1 USB interface, 1 GPIO module, 1 WDT module, 4 32-bit Timers, 1 CRC module, 2 SPI interfaces, 2 UART interfaces, and one I2C interface.

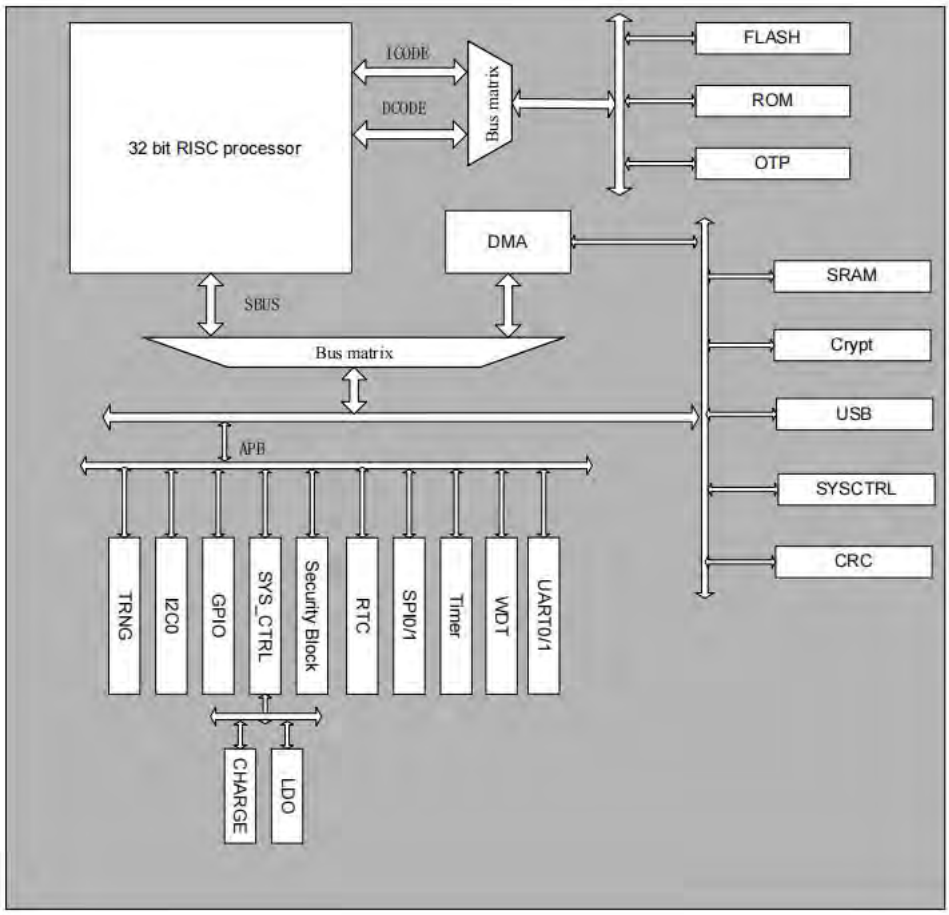


Figure 1 System block diagram

2 Characteristics

2.1 Electrical Characteristics

Table 1 Ultimate Parameters

Parameters	Note	Range	Unit
VDD33	LDO output voltage	● VCC >= 3.3 ■ 3.2~3.3 ● VCC >= 2.1 and VCC <3.2 ■ 2~3.1	V
IddLdodrive	LDO drive current	150	mA
Iddpd	Shutdown current	--	nA
Tamb	Operating temperature	-40~+85	℃
Tstg	Storage temperature	-40~+125	℃

Parameters	Note	Range	Unit
Ground	Ground	-0.3~0.3	V
Voh	Digital output high level	VDD -0.3 ~ VDD+0.3	V
Vol	Digital output low level	<0.4	V
Ioh	Source current	2/4/8/12	mA
Iol	Sink current	2/4/8/12	mA
Vih	Digital input high level	≥0.7×VDD	V
ViL	Digital input low level	≤0.3×VDD	V

Table 2 Electrical Characteristics

Parameters	Condition (-40°C to +85°C)	Value		Unit
		Minimum	Maximum	
VCC		2.2	5.6	V
CHARGE_VCC		4.5	5.6	V
VDD33		2.2	3.6	V
VBAT33		1.8	3.6	V
Vol	VDD=3.3V	-	0.4	V
Voh	VDD=3.3V	VDD – 0.3	-	V
VIH	VDD=3.3V	0.7×VDD	-	V
VIL	VDD=3.3V	-	0.3×VDD	V

Table 3 Safety-related Characteristics

Sensor	Note	Range	Unit
Temperature sensor	High temperature detection range	100±15	℃
	Low temperature detection range	-30 ~ -40	℃
Voltage sensor	High voltage detection range of main power voltage	5.5±0.1	V
	Low voltage detection range of main power voltage	2.0±0.1	V
Clock frequency sensor	32K clock frequency detection range	32±50%	KHz

Table 4 List of Power Consumption

Operating Mode	Note	Power consumption	Unit
RUN	● All peripherals are turned on ■ @80MHz ■ @48MHz ● All peripherals are turned off ■ @80MHz ■ @48MHz(turn on USB)	 22 19 8 16	mA
CPU Sleep	All peripherals are turned off @80MHz	3.5	mA
Deep Sleep	Support IO、PowerKey、USB 、RTC、SPI、UART wake-up	200	uA

Operating Mode	Note	Power consumption	Unit
VBAT33	● Main power down ● Main power on with AVD33 – VBAT > 0.3V	1.7 0.4	uA

Table 5 Charging module related parameters

Program Resistor Value	Trickle Charge Current(mA)	Trickle Threshold(V)	Constant current charging current(mA)	Charging voltage(V)
1K	19±1	2.87±0.01	100	4.15±.0.05
2K	10±1	2.88±0.01	50	4.15±.0.05

2.2 Definition of pins

2.2.1 QFN32

Table 6 Definitions of MH1706 QFN32 4mm×4mm Packaging Pins

PIN No.	PIN name	ALT0	ALT1 (default)	ALT2	ALT3	Remark
1	CHARGE_VCC					CHARGE power input
2	CHARGE_VBAT					CHARGE power output，connect to the battery
3	CHARGE_VPROG					CHARGE current control pin
4	RST_N					
5	PB1	UART0_TX	PB[1]	SPI0_CSN0	PWM1	
6	PB3	UART0_RTS	PB[3]	SPI0_MISO	PWM3	
7	PB0	UART0_RX	PB[0]	SPI0_SCK	PWM0	
8	PB2	UART0_CTS	PB[2]	SPI0_MOSI	PWM2	
9	PA13	UART1_TX	PA[13]	SPI0_CSN0	PWM1	
10	PA15	UART1_RTS	PA[15]	SPI0_MISO	PWM3	
11	PA11	I2C0_SDA				
12	PA10	I2C0_SCL				
13	PA14	UART1_CTS	PA[14]	SPI0_MOSI	PWM2	
14	PA12	UART1_RX	PA[12]	SPI0_SCK	PWM0	
15	VDD33					5V to 3.3V output
16	DP					USB DP
17	DN					USB DN
18	**GND**					Ground
19	PA5	SWDATA		UART1_TX		
20	PA4	SWCLK		UART1_RX		

PIN No.	PIN name	ALT0	ALT1 (default)	ALT2	ALT3	Remark
21	PB7	SPI1_MISO	PB[7]	UART0_RTS	PWM0	
22	PB6	SPI1_MOSI	PB[6]	UART0_CTS		
23	PB5	SPI1_CSN	PB[5]	UART0_TX		
24	PB4	SPI1_CLK	PB[4]	UART0_RX		
25	VDD33					5V to 3.3V output
26	VCC					5V to 3.3V LDO input
27	POWER_KEY					Switch button
28	PA6	SPI0_SCK	PA[6]	UART1_RX	PWM0	
29	PA3	UART0_RTS	PA[3]	SPI0_MISO	PWM3	
30	PA2	UART0_CTS	PA[2]	SPI0_MOSI	PWM2	
31	PA1	UART0_TX	PA[1]	SPI0_CSN0	PWM1	
32	PA0	UART0_RX	PA[0]	SPI0_SCK	PWM0	

2.2.2 QFN20

Table 7Definitions of MH1706 QFN20 4mm×4mm Packaging Pins

PIN No.	PIN name	ALT0	ALT1 (default)	ALT2	ALT3	Remark
1	VCC					Power input
2	PA13	UART1_TX	PA[13]	SPI0_CSN0	PWM1	
3	PA15	UART1_RTS	PA[15]	SPI0_MISO	PWM3	
4	PA12	UART1_RX	PA[12]	SPI0_SCK	PWM0	
5	PA10	I2C0_SCL				
6	PA11	I2C0_SDA				
7	PA14	UART1_CTS	PA[14]	SPI0_MOSI	PWM2	
8	DN					USB DN
9	DP					USB DP
10	VDD33					
11	**GND**					
12	PA5	SWDATA		UART1_TX		
13	PA4	SWCLK		UART1_RX		
14	XO32K					XTAL 32KHz Output
15	XI32K					XTAL 32KHz Input
16	VBAT33					Battery power supply
17	PA9	SPI0_MISO	PA[9]	UART1_RTS	PWM3	
18	PA2	UART0_CTS	PA[2]	SPI0_MOSI	PWM2	
19	PA1	UART0_TX	PA[1]	SPI0_CSN0	PWM1	
20	PA0	UART0_RX	PA[0]	SPI0_SCK	PWM0	

2.2.3 DFN8

Table 8 Definitions of MH1706 DFN8 3mm×3mm Packaging Pins

PIN No.	PIN name	ALT0	ALT1 (default)	ALT2	ALT3	Remark
1	VCC1					short connection with VCC
2	PA11	I2C0_SDA				
3	PA10	I2C0_SCL				
4	VCC					Power input
5	PA3	UART0_RTS	PA[3]	SPI0_MISO	PWM3	
6	PA2	UART0_CTS	PA[2]	SPI0_MOSI	PWM2	
7	PA1	UART0_TX	PA[1]	SPI0_CSN0	PWM1	
8	PA0	UART0_RX	PA[0]	SPI0_SCK	PWM0	

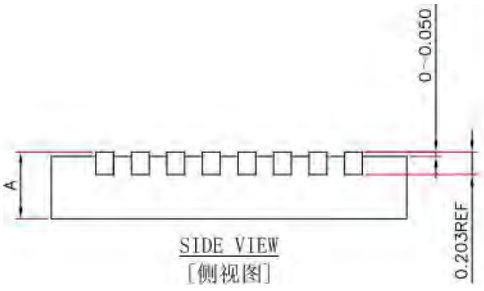
2.2.4 SOP8

Table 9 Definitions of MH1706 SOP8 Packaging Pins

PIN No.	PIN name	ALT0	ALT1 (default)	ALT2	ALT3	Remark
1	PA0	UART0_RX	PA[0]	SPI0_SCK	PWM0	
2	PA1	UART0_TX	PA[1]	SPI0_CSN0	PWM1	
3	PB2	UART0_CTS	PB[2]	SPI0_MOSI	PWM2	
4	**GND**					Ground
5	PA11	I2C0_SDA				
6	PA10	I2C0_SCL				
7	PA9	SPI0_MISO	PA[9]	UART1_RTS	PWM3	
8	**VCC**					Power input

2.3 Information on package

2.3.1 QFN32



	MIN.	NORM.	MAX.
A	0.800	0.850	0.900

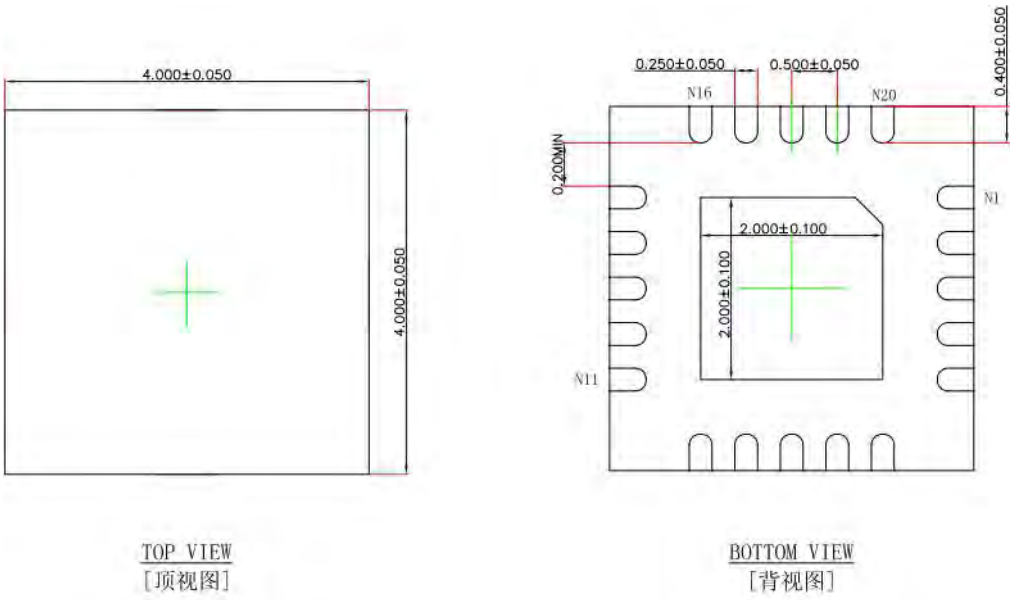


Figure 2 MH1706QFN32 4mm×4mm package dimension

2.3.2 QFN20

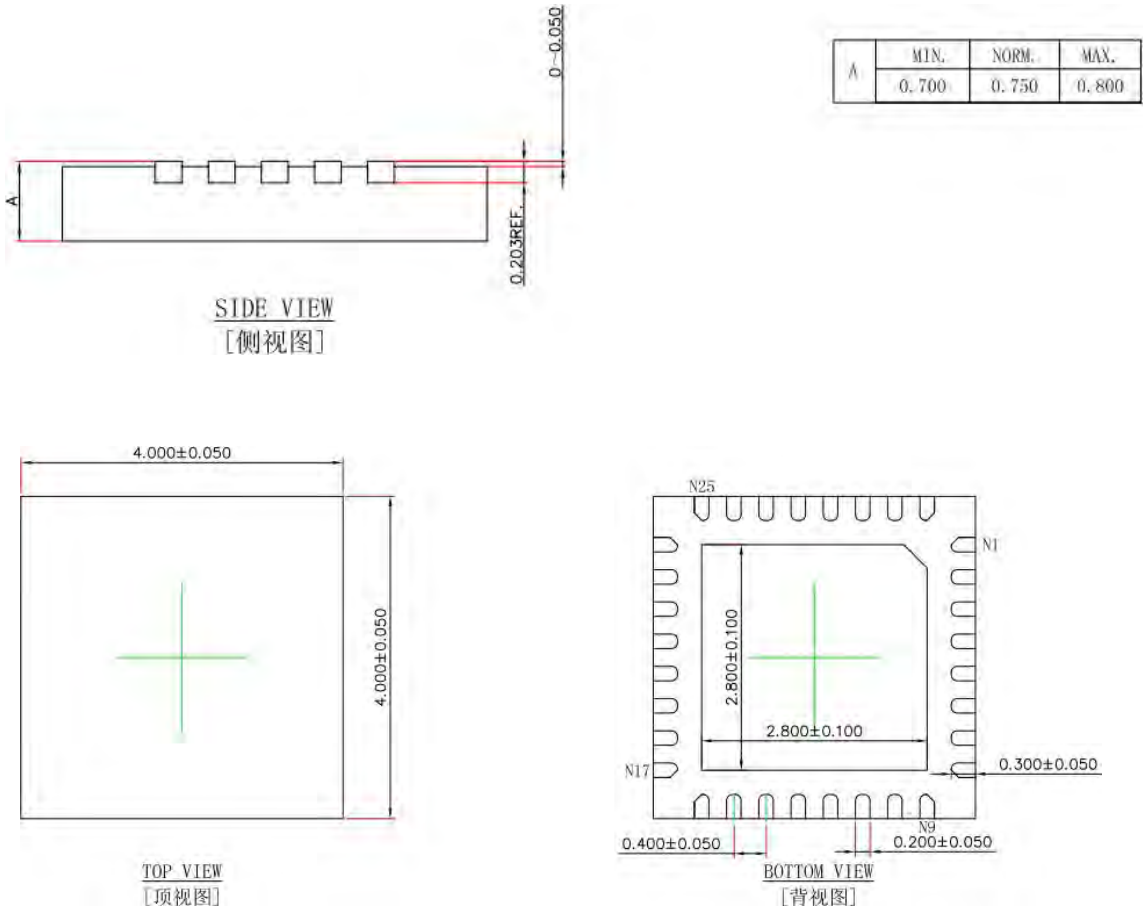
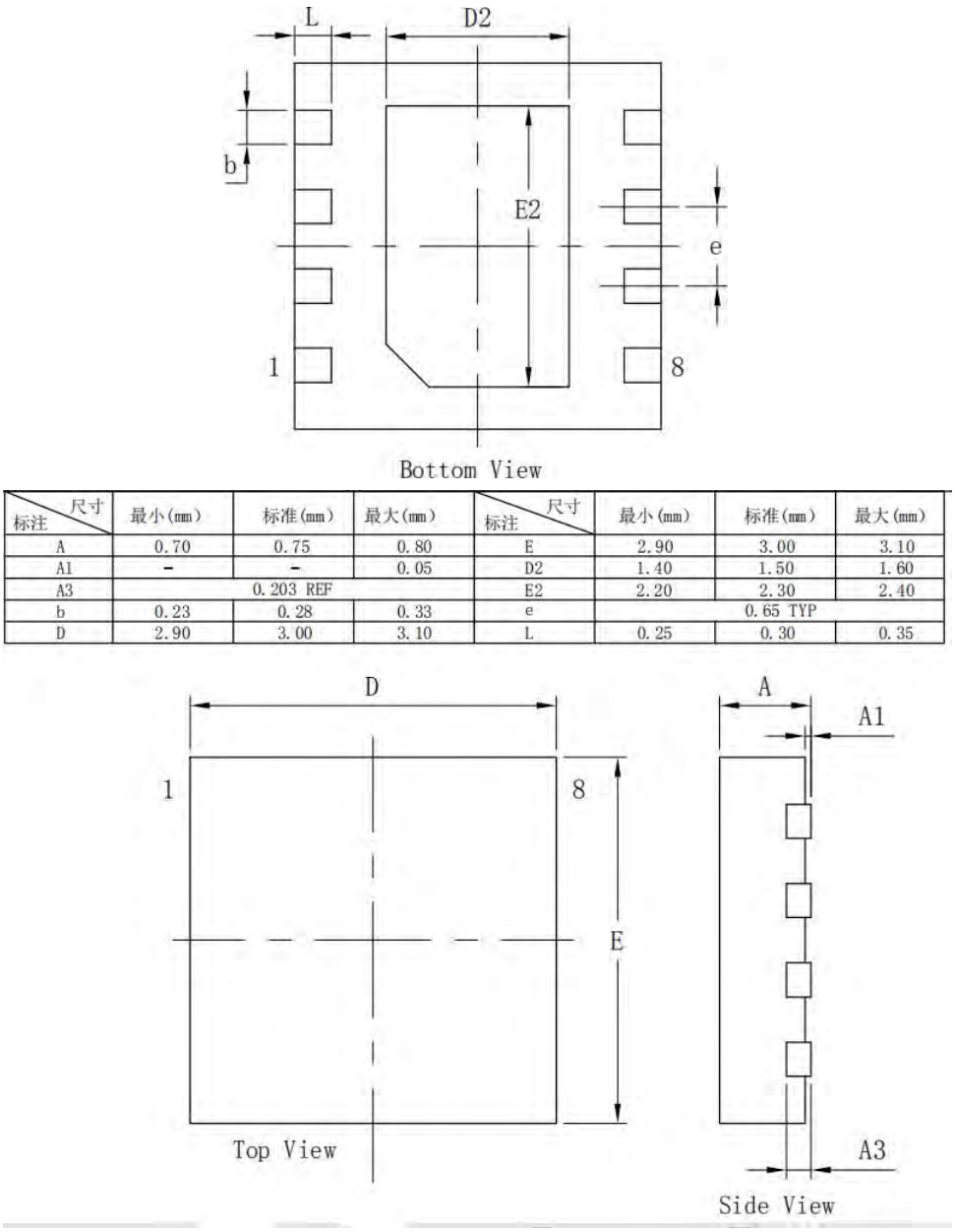


Figure 3 MH1706 QFN20 4mm×4mm package dimension

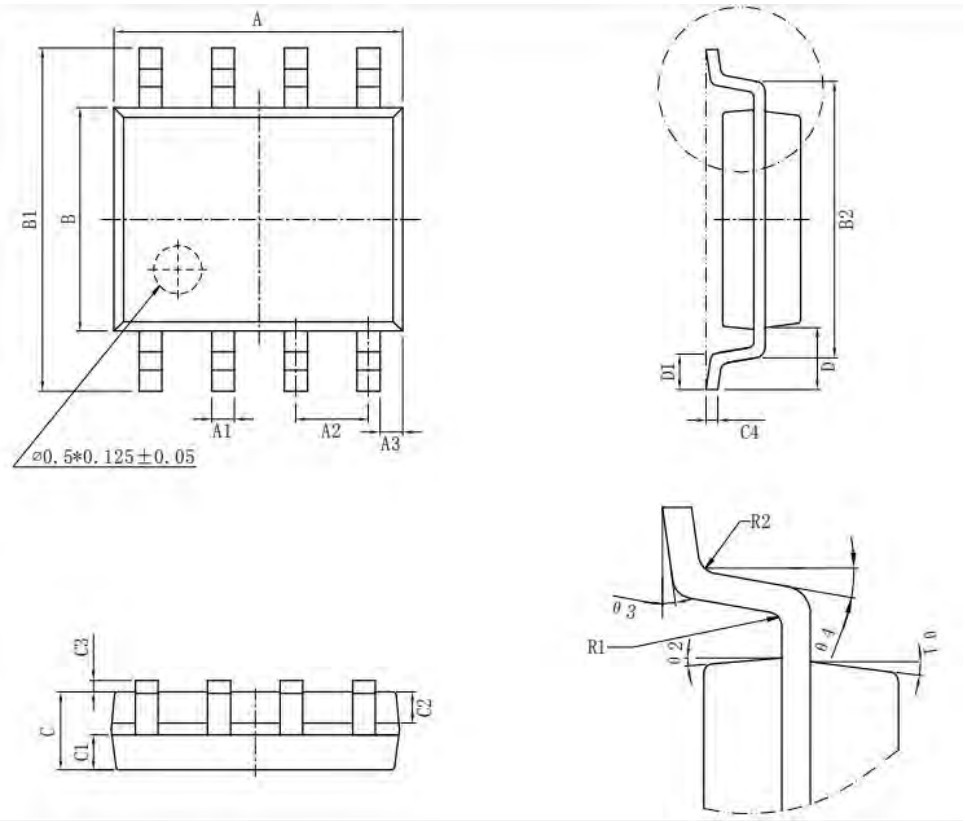
2.3.3 DFN8



尺寸 / 标注	最小(mm)	标准(mm)	最大(mm)	尺寸 / 标注	最小(mm)	标准(mm)	最大(mm)
A	0.70	0.75	0.80	E	2.90	3.00	3.10
A1	-	-	0.05	D2	1.40	1.50	1.60
A3	0.203 REF			E2	2.20	2.30	2.40
b	0.23	0.28	0.33	e	0.65 TYP		
D	2.90	3.00	3.10	L	0.25	0.30	0.35

Figure 4 MH1706 DFN8 3mm×3mm package dimension

2.3.4 SOP8



标注 \ 尺寸	最小(mm)	最大(mm)	标注 \ 尺寸	最小(mm)	最大(mm)
A	4.80	5.00	C3	0.05	0.20
A1	0.356	0.456	C4	0.203	0.233
A2	1.27TYP		D	1.05TYP	
A3	0.345TYP		D1	0.40	0.80
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
B2	5.00TYP		θ1	17° TYP4	
C	1.30	1.60	θ2	13° TYP4	
C1	0.55	0.65	θ3	0° ~ 8°	
C2	0.55	0.65	θ4	4° ~ 12°	

Figure 5 MH1706 SOP8 150mil package dimension

2.4 Ordering Information on part numbers

Table 10 MH1706 part numbers

Ordering Information (Part Numbers)	SRAM	Flash	Package
MH1706Q35UE00	32KB	384KB	QFN32
MH1706Q25UE00	32KB	384KB	QFN20
MH1706D15UE00	32KB	384KB	DFN8
MH1706S15UE00	32KB	384KB	SOP8

3 Details of Functional Modules

3.1 Description of peripherals

3.1.1 SPI

MH1706 provides 1 SPI master/slave and 1 SPI master device interfaces, which can support communication with multiple slave devices when used as the master device interface.

Characteristics of SPI peripherals:

- Operation of Master mode and Slave mode at independent address
- Master mode supports full duplex, simplex receiving, simplex transmitting and EEPROM mode
- Multiple Master conflict detections
- Support three communication modes including Motorola SPI, Texas Instruments SPI, and National Semiconductor Microwire
- Receive and transmit FIFO independently at the depth of 16 and the fixed width of 16 bits
- The frame length is configurable, ranging from 4 to 16 bits
- DMA interface

The common Motorola SPI communication protocol supports four communication modes, so as to achieve full duplex communication. The default mode 0 is used to power on the system.

The four communication formats as specified in SPI protocol are described as follows:

- Mode 0: Clock polarity (CPOL) = 0, clock phase (CPHA) = 0. In this mode, the idle state of the serial synchronous clock is low. MH1706 samples data on the clock's first rising edge. This mode is default mode.
- Mode 1: Clock polarity (CPOL) = 0, clock phase (CPHA) = 1. In this mode, the idle state of the serial synchronous clock is low. MH1706 samples data on the clock's second falling edge;
- Mode 2: Clock polarity (CPOL) = 1, clock phase (CPHA) = 0. In this mode, the idle state of the serial synchronous clock is high. MH1706 samples on the clock’s first falling edge.
- Mode 3: Clock polarity (CPOL) = 1, clock phase (CPHA) = 1. In this mode, the idle state of the serial synchronous clock is high. MH1706 samples data on the clock’s second rising edge.

Note: In order to keep the normal operation of the MH1706 SPI, ensure that the CSN signal line is kept at a high level during mode switching. At the same time, when the master thinks that the slave has an error during the communication process, it can restore the slave

to normal by pulling CSN high.

SPI interfaces are described as follows:

- SCK: The clock input pin of SPI; when the communication rate of 200K is adopted, the delay of 20us is needed between the bytes as a minimum;
- CSN: MH1706 selection signal of SPI, which is the input pin of MH1706, with low efficiency;
- MOSI: The data input pin of SPI;
- MISO: The data output pin of SPI.

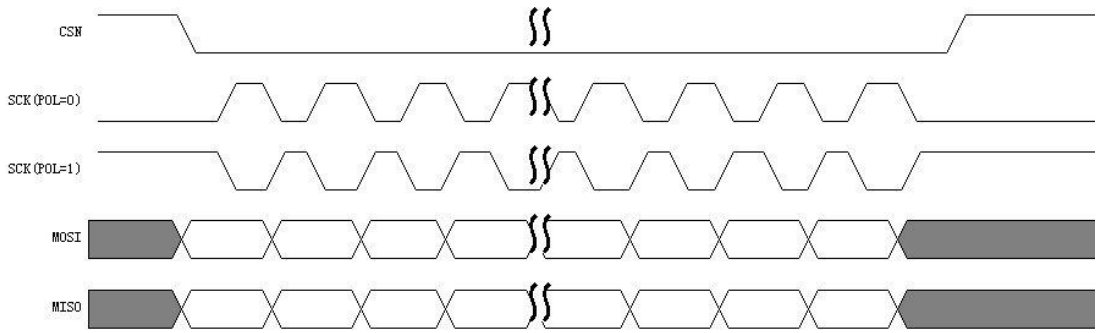


Figure 6 SPI Time Sequence 1 (CPHA=0)

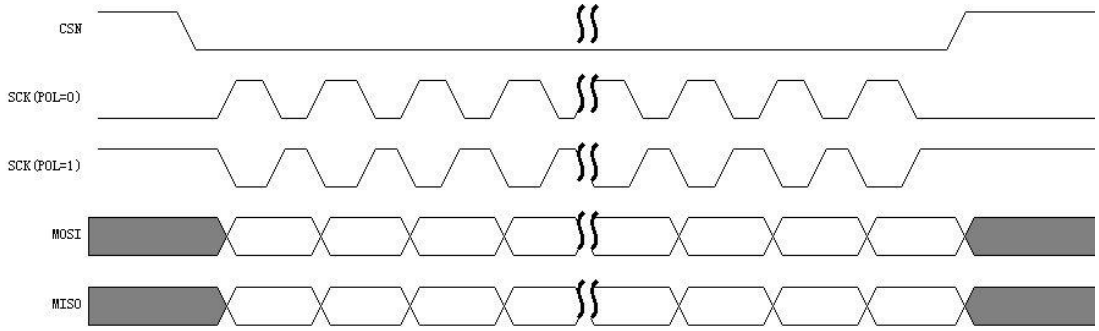


Figure 7 SPI Time Sequence 2(CPHA=1)

3.1.2 UART

MH1706 has two full-duplex UART serial communication interfaces, which all support 4-wire mode.

Characteristics of UART peripherals:

- Receive and transmit FIFO independently at the depth of 16 bytes;
- Control of FIFO enabling
- Setting of data bits, supporting 5-8bit
- Forced output of 9 check bits
- Frame error, check error, break interrupt detection

- IrDA 1.0 infrared protocol support
- DMA receiving

UART peripherals support independent receiving and transmitting of FIFO, and FIFO function can be configured for use by enabling bits.

The receiving and transmitting of FIFO by UART supports the full interrupt in receiving FIFO and the empty interrupt in transmitting FIFO respectively, and the trigger values thereof are configurable. The interrupt source in transmitting FIFO shares the same interrupt source with the transmitter holding register empty (THRE) in the non-FIFO mode, which is set by the software.

3.1.3 USB

USB2.0 Device, support high-speed and full-speed mode.

USB peripherals support USB suspend/resume operation, which can stop the device clock for low power consumption.

- Compliance with the technical specifications of USB2.0 high-speed/full-speed device
- Support 4 bidirectional endpoints (including control endpoint)
- A total of 512 bytes of endpoint cache FIFO, of which 384 bytes can be configured to different endpoints as needed
- All endpoints share receive FIFO, optional share transmit FIFO
- Support Buffer DMA with FIFO and RAM to automatically send and receive data
- Includes an internal high-speed/full-speed USB PHY that automatically calibrates the clock according to the host communication SOF packet

3.1.4 Sensor

MH1706 has built-in multiple environmental safety detection circuits, including:

- Clock frequency detection
- High and low temperature attack detection
- High and low voltage attack detection
- Light detection
- Active shielding
- Voltage glitch detection

3.1.5 GPIO

MH1706 supports up to 24 GPIOs, and each IO multiplexes pins with peripherals. Each GPIO can be configured as input, output, and interrupt mode; when GPIO is configured as output, each IO output value can be configured separately. IO supports strong push-pull/open-drain output modes.

3.1.6 DMA

Direct memory access (DMA) is used to provide high-speed data transmission between peripherals and memory or between memory and memory. Data can be moved quickly through DMA without CPU intervention, so as to free up CPU resources for other operations.

The DMA controller has eight channels, each of which is specially used to manage the requests for access from memory to memory, from memory to peripheral, and from peripheral to memory. The setting of independent priority is assigned to each channel.

The main characteristics include:

- 2 independent configurable channels
- 2 independent hardware DMA requests (DMA hard handshake interface), each channel also supports software departure (DMA soft handshake interface)
- Support multi-width data transmission
- Each channel has its own interrupt signal and flag
- Support the transmission from memory to memory, from memory to peripheral, and from peripheral to memory