LPDDR5X SDRAM Component

Version 1.1

June 16, 2026

LPDDR5X-8533 | 1.05V

64Gb

Revision History

Revision	Date	Description	Editor
1.0	Feb.06,2025	Initial release	Danny Lu
1.1	June 16, 2026	Remove LPDDR5X SDRAM addressing for 8B mode	Pei Yu Shih

1.0 Specifications

Part No.	L5EG32D4023MCAS
Configuration	2048M x 32
Product Code	LPDDR5X
Density	64 Gigabit (4 Die)
VDD1/VDD2/VDDQ	1.8V / 1.05V / 0.5V
FBGA package (Pb and halogen free)	315-ball (12.4mm x 15.0mm)
Speed	8533Mbps (tWCK=0.23ns)
Operating temperature	-25° ~ 85°C

2.0 Features

- VDD1 = 1.8V (1.70V ~ 1.95V)
- VDD2H = 1.05V (1.01V ~ 1.12V)
- VDD2L = VDD2H or 0.9V (0.87V ~ 0.97V)
- VDDQ = 0.5V (0.47V ~ 0.57V)
- Configuration 2048 M x 32 (2channels x16 I/O)
- Single x16 channel/die
- Double-data-rate command/address entry
- Differential command clocks (CK_t/CK_c) for high-speed operation
- Differential data clocks (WCK_t/WCK_c)
- Optional differential read strobe (RDQS_t/RDQS_c)
- 16n-bit or 32n-bit prefetch architecture
- Bank Architecture: Bank Group (BG) mode, and 16-bank (16B) mode supported
- Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
- Background ZQ calibration/command-based ZQ calibration
- Optional link protection (link ECC)
- Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- Interface LVSTL0.5/0.3 I/O
- I/O type: Low-swing single-ended, VSS terminated
- VOH-compensated output drive
- Programmable VSS on-die termination (ODT)
- Non target ODT support
- Dynamic voltage frequency scaling for VDDQ (DVFSQ) support
- Per byte and per pin DFE support
- Dynamic voltage frequency scaling core (DVFSC) support
- Single-ended CK, single-ended WCK and single-ended RDQS
- Optional Data copy and Write X
- JEDEC JESD209-5 compliant

3.0 LPDDR5 SDRAM Package, Pinout Description and Addressing

3.1 LPDDR5 SDRAM 2CHX32 Ballout using MO-338A

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	NC	NC	VDDQ	DMI0_A	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DMI1_A	VDDQ	NC	NC
B	NC	VDDQ	RDQS0_T_A	VSS	DQ4_A	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ12_A	VSS	RDQS1_T_A	VDDQ	NC
C	VDD1	DQ1_A	VDDQ	RDQS0_C_A	VSS	DQ5_A	VDD2H	VSS	VDD2H	DQ13_A	VSS	RDQS1_C_A	VDDQ	DQ9_A	VDD1
D	DQ0_A	VSS	DQ3_A	VDDQ	WCK0_C_A	VSS	VSS	VDD2H	VSS	VSS	WCK1_C_A	VDDQ	DQ11_A	VSS	DQ8_A
E	VSS	DQ2_A	VSS	WCK0_T_A	VDDQ	DQ6_A	VDD2H	VSS	VDD2H	DQ14_A	VDDQ	WCK1_T_A	VSS	DQ10_A	VSS
F	VDDQ	VSS	VDDQ	VDDQ	DQ7_A	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ15_A	VDDQ	VDDQ	VSS	VDDQ
G	VDDQ	VDDQ	VSS	CA0_A	VSS	CS1_A	VSS	CA2_A	VSS	CA4_A	VSS	CA6_A	VSS	VDDQ	VDDQ
H	Reset_N	VDD2L	VSS	VSS	CA1_A	VSS	CS0_A	VSS	CK_t_A	VSS	CA3_A	VSS	CA5_A	VDD2L	ZQ_A
J	VSS	VDD2L	VSS	RFU	VDD2H	RFU	VSS	VSS	CK_c_A	VSS	VDD2H	VSS	VSS	VDD2L	VSS
K	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H
L	VSS	VSS	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VSS	VSS
M	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H
N	VSS	VDD2L	VSS	VSS	VDD2H	VSS	CK_c_B	VSS	VSS	VSS	VDD2H	VSS	VSS	VDD2L	VSS
P	RFU	VDD2L	CA5_B	VSS	CA3_B	VSS	CK_t_B	VSS	CS0_B	VSS	CA1_B	VSS	VSS	VDD2L	RFU
R	VDDQ	VDDQ	VSS	CA6_B	VSS	CA4_B	VSS	CA2_B	VSS	CS1_B	VSS	CA0_B	VSS	VDDQ	VDDQ
T	VDDQ	VSS	VDDQ	VDDQ	DQ15_B	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ7_B	VDDQ	VDDQ	VSS	VDDQ
U	VSS	DQ10_B	VSS	WCK1_t_B	VDDQ	DQ14_B	VDD2H	VSS	VDD2H	DQ6_B	VDDQ	WCK0_T_B	VSS	DQ2_B	VSS
V	DQ8_B	VSS	DQ11_B	VDDQ	WCK1_c_B	VSS	VSS	VDD2H	VSS	VSS	WCK0_C_B	VDDQ	DQ3_B	VSS	DQ0_B
W	VDD1	DQ9_B	VDDQ	RDQS1_C_B	VSS	DQ13_B	VDD2H	VSS	VDD2H	DQ5_B	VSS	RDQS0_C_B	VDDQ	DQ1_B	VDD1
Y	NC	VDDQ	RDQS1_T_B	VSS	DQ12_B	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ4_B	VSS	RDQS0_T_B	VDDQ	NC
AA	NC	NC	VDDQ	DMI1_B	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DMI0_B	VDDQ	NC	NC

Note(s):

1. 0.8 mm pitch (X-axis) 15 columns, 0.7 mm pitch (Y-axis), 21 rows.

2. Top View, A1 in top left corner.

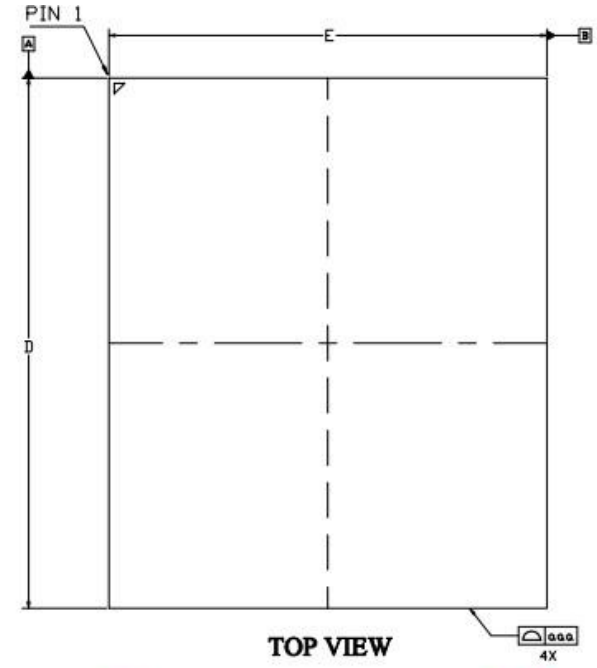
3.2 Pad Definition and Description

Symbol	Type	Description	Note
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) Command/Address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising(falling) edge of CK_t (CK_c) and second crossing point is falling(rising) edge of CK_t (CK_c). Single Data Rate (SDR) inputs, CS is sampled on the crossing point that is the rising(falling) edge of CK_t (CK_c).	
CS[1:0]	Input	**Chip Select:** CS is part of the command code and is sampled on the rising(falling) edge of CK_t (CK_c) unless the device is in power-down or Deep Sleep mode where it becomes an asynchronous signal.	
CA[6:0]	Input	**Command/Address Inputs:** CA signals provide the Command and Address input according to the Command Truth Table.	
DQ[15:0]	I/O	**Data Input/Output:** Bi-direction data bus.	
WCK[1:0]_t WCK[1:0]_c	Input	**Data Clocks:** WCK_t and WCK_c are differential clocks used for WRITE data capture and READ data output.	
RDQS [1:0]_t , RDQS[1:0]_c	RDQS_t:I/O, RDQS_c: Output	**Read Data Strobe:** RDQS_t and RDQS_c are the differential output clock signals used to strobe data during a READ operation. And RDQS_t is also used as a Parity pin at Write with Link Protection enabled.	1
DMI[1:0]	I/O	**Data Mask Inversion:** DMI achieves multiple function such as Data Mask (DM), Data Bus Inversion (DBI), and Parity at read with ECC operation by setting the Mode Register and DMI is a bi-directional signal and each byte of data has a DMI signal.	1
ZQ	Reference	**ZQ:** ZQ is used to calibrate the output drive strength and the termination resistance as calibration reference. There is one ZQ pad per die. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.	
VDDQ,VDD1, VDD2H,VDD2L	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.	
VSS	GND	**Ground Reference:** Power supply ground reference.	
RESET_n	Input	**RESET:** When asserted LOW, the RESET_n signal resets the die. RESET_n is an asynchronous signal.	
NC	—	**No connect:** Not internally connected.	
RFU	—	**Reserved for Future Use**: Not internally connected.	

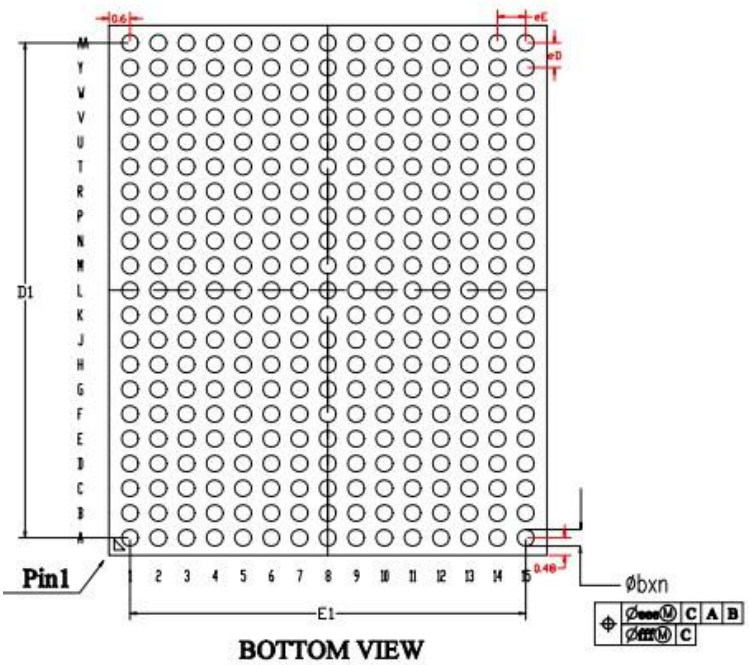
Note(s):

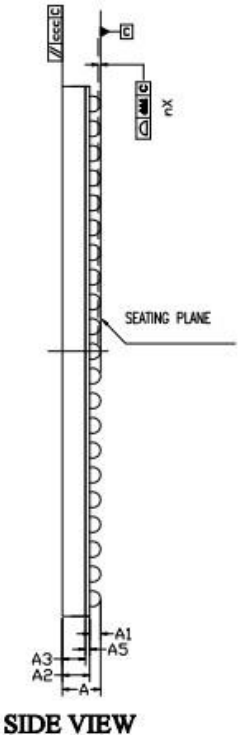
(1) See e Table Pins Per-Byte Signal List/Description for Link Protection disabled and Pins Per-Byte Signal List/Description for Link Protection enabled Per-Byte Signal List/Description for multi-function definition for these pins.

3.3 Package Dimension : 315Ball Fine Pitch Ball Grid Array Outline



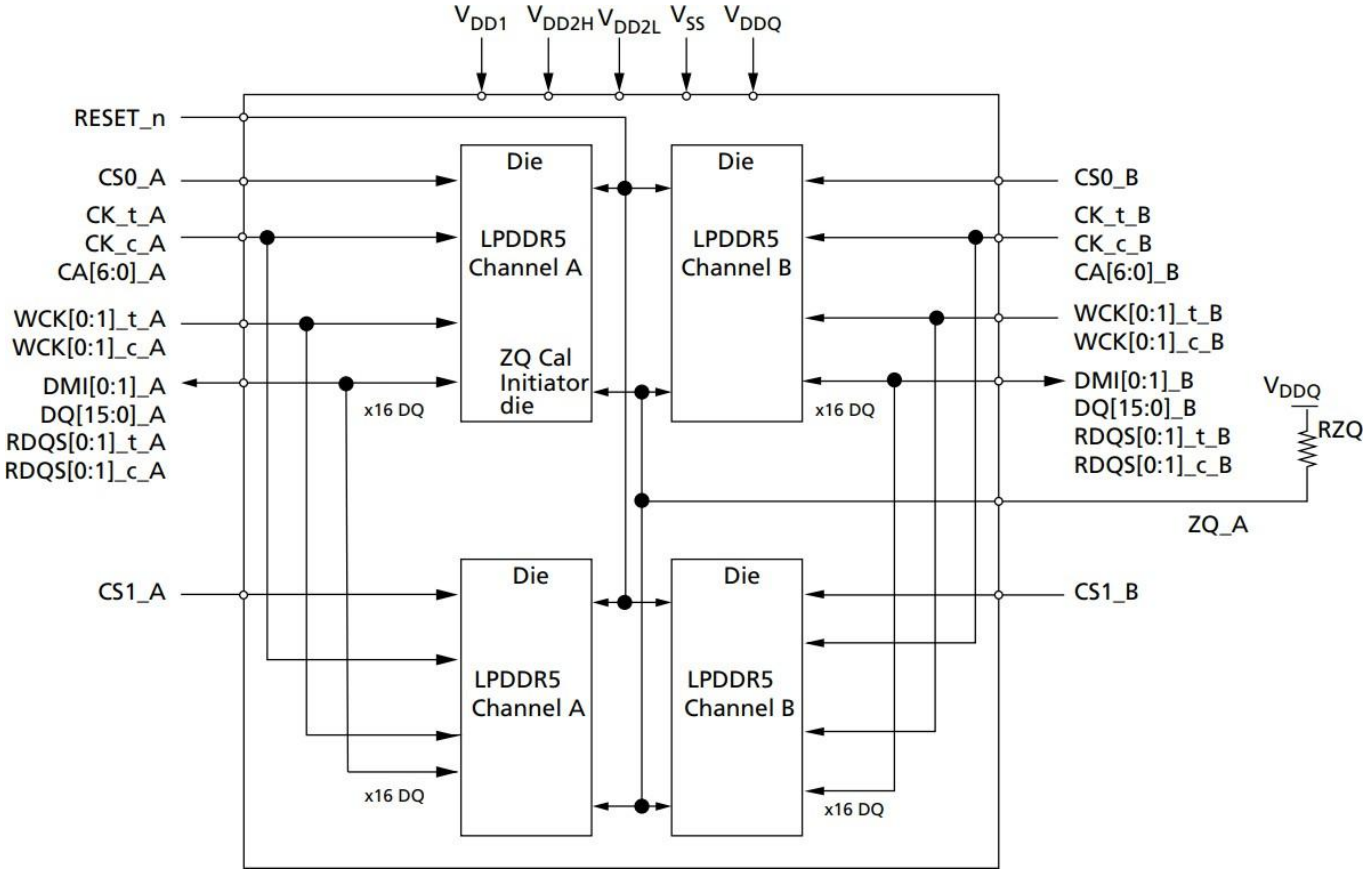
	Symble	Dimension in mm			Dimension in inch		
		Min	Normal	Max	Min	Normal	Max
TOTAL THICKNESS	A	---	0.990	1.100	---	0.0390	0.0433
STAND OFF	A1	0.250	0.280	0.310	0.0098	0.0110	0.0122
SBT+MOLD THICKNESS	A2	0.670	0.710	0.750	0.0264	0.0280	0.0295
MOLD THICKNESS	A3	0.390	0.420	0.450	0.0154	0.0165	0.0177
SUBSTRATE THICKNESS	A5	0.260	0.290	0.320	0.0102	0.0114	0.0126
BALL WIDTH	Φb	0.430	0.480	0.530	0.0169	0.0189	0.0209
BALL PITCH	eD		0.700			0.0276	
	eE		0.800			0.0315	
BALL COUNT	n			315			
BODY SIZE	D	14.900	15.000	15.100	0.5866	0.5906	0.5945
	E	12.300	12.400	12.500	0.4843	0.4882	0.4921
EDGE BALL CENTER TO CENTER	D1	13.900	14.000	14.100	0.5472	0.5512	0.5551
	E1	11.100	11.200	11.300	0.4370	0.4409	0.4449
PKG EDGE TOLERANCE	aaa		0.100			0.0039	
MOLD FLATNESS	ccc		0.100			0.0039	
COPLANARITY	ddd		0.100			0.0039	
BALL OFFSET(PACKAGE)	eee		0.150			0.0059	
BALL OFFSET(BALL)	fff		0.050			0.0020	
JEDEC				MO-338(REF)			





3.4 Functional Block Diagram

Quad-Die, Dual-Channel, Dual-Rank



4.0 Functional Description

LPDDR5 SDRAM is a high-speed synchronous DRAM device internally configured as 4Bank/4BG per channel. LPDDR5 SDRAM's density is up to 32Gb.

These devices contain the following number of bits:
2Gb has 2,147,483,648 bits.
3Gb has 3,221,225,472 bits.
4Gb has 4,294,967,296 bits.
6Gb has 6,442,450,944 bits.
8Gb has 8,589,934,592 bits.
12Gb has 12,884,901,888 bits.
16Gb has 17,179,869,184 bits.
24Gb has 25,769,803,776 bits.
32Gb has 34,359,738,368 bits.

LPDDR5 devices use 1 or 2 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 7 bit CA bus contains command, address, bank information and functional indicators. Each command uses 1 or 2 clock cycle, during which command information is transferred on the rising and the falling edge of the clock. See Command Truth Table for details.
These devices use double data rate architecture on the DQ pins to achieve high speed operation in WCK clocking system. The double data rate architecture is essentially 16n pre-fetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR5 SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and 16 corresponding n-bit wide, one half-clock-cycle data transfer at the I/O pins. Read and Write accesses to the LPDDR5 SDRAMs are burst oriented; accesses start a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is followed by Read, Write or Mask Write command.
The address and BA bits registered coincident with the Activate command are used to select the row and the bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the bank and the starting column location for the burst access.
Prior to normal operation, the LPDDR5 SDRAM is required to be initialized. The Power-Up, Initialization, and Power-off Procedure section provides detailed information covering device initialization.

4.1 LPDDR5 SDRAM Addressing

4.1.1 LPDDR5 SDRAM x16 mode Addressing for BG Mode (4Banks/4Bank Groups)

Memory Density	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Configuration	8Mb x16DQ x 4 BG x 4 banks	12Mb x16DQ x 4 BG x 4 banks	16Mb x16DQ x 4 BG x 4 banks	24Mb x16DQ x 4 BG x 4 banks	32Mb x16DQ x 4 BG x 4 banks	48Mb x 16DQ x 4 BG x 4 banks	64Mb x 16DQ x 4 BG x 4 banks	96Mb x 16DQ x 4 BG x 4 banks	128Mb x 16DQ x 4 BG x 4 banks
Number of Banks in BG	4	4	4	4	4	4	4	4	4
Number of Bank Groups	4	4	4	4	4	4	4	4	4
Array Pre-Fetch	256	256	256	256	256	256	256	256	256
Number of Rows	8,192	12,288	16,384	24,576	32,768	49,152	65,536	98,304	131,072
Number of Columns(fetchboundaries)	64	64	64	64	64	64	64	64	64
PageSize (Bytes)	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048
Density	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank Address	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1	BA0 - BA1
Bank Group Addresses	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1	BG0 - BG1
Row Addresses	R0 - R12	R0 - R13 (R12=0 when R13=1)	R0 - R13	R0 - R14 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	R0 - R16 (R15=0 when R16=1)	R0 - R16
Column Addresses	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5
Burst Addresses	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3

Memory Density	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Burst Starting Address Boundary	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit
Native Burst Length	16	16	16	16	16	16	16	16	16

Note(s):

(1) The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.

(2) Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.

(3) For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

(4) A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.

4.1.2 LPDDR5 SDRAM x16 mode Addressing for 16B Mode

Memory Density	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Configuration	8Mb x 16DQ x 16 banks	12Mb x 16DQ x 16 banks	16Mb x 16DQ x 16 banks	24Mb x 16DQ x 16 banks	32Mb x 16DQ x 16 banks	48Mb x 16DQ x 16 banks	64Mb x 16DQ x 16 banks	96Mb x 16DQ x 16 banks	128Mb x 16DQ x 16 banks
Number of Banks	16	16	16	16	16	16	16	16	16
Array Pre-Fetch	256	256	256	256	256	256	256	256	256
Number of Rows	8,192	12,288	16,384	24,576	32,768	49,152	65,536	98,304	131,072
Number of Columns (fetch boundaries)	64	64	64	64	64	64	64	64	64
Page Size (Bytes)	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048	2,048
Density	2,147,483,648	3,221,225,472	4,294,967,296	6,442,450,944	8,589,934,592	12,884,901,888	17,179,869,184	25,769,803,776	34,359,738,368
Bank Address	BA0 - BA3	BA0 - BA3	BA0 - BA3	BA0 - BA3	BA0 - BA3	BA0 - BA3	BA0 - BA3	BA0 - BA3	BA0 - BA3
Row Addresses	R0 - R12	R0 - R13 (R12=0 when R13=1)	R0 - R13	R0 - R14 (R13=0 when R14=1)	R0 - R14	R0 - R15 (R14=0 when R15=1)	R0 - R15	R0 - R16 (R15=0 when R16=1)	R0 - R16
Column Addresses	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5	C0-C5
Burst Addresses	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3	B0-B3

Memory Density	2Gb	3Gb	4Gb	6Gb	8Gb	12Gb	16Gb	24Gb	32Gb
Burst Starting Address Boundary	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit	128-bit
Native Burst Length	16	16	16	16	16	16	16	16	16

Note(s):

(1) The lower three burst addresses (B0-B2) are assumed to be "zero" and are not transmitted on the CA bus.

(2) Row and Column address values on the CA bus that are not used for a particular density must be at valid logic levels.

(3) For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

(4) A row address input that violates the restriction described in Note 3 may result in undefined or vendor specific behavior. Consult the memory vendor for more information.

4.2 Refresh Requirement Parameters

Parameter		Symbol	16Gb Die BG & 16B Mode	Units	Notes
Refresh Window (tREFW) (1x Refresh)[2,3]		tREFW	32	ms	
Required Number of REFRESH Commands in a tREFW window		R	8192		
Average Refresh Interval(1x Refresh)[2]	REFab	tREFI	3.906	µs	
	REFpb	tREFipb	488	ns	
Refresh Cycle Time (All Banks)		tRFCab	280	ns	3
Refresh Cycle time (Per Bank)		tRFCpb	140	ns	3
Per-bank Refresh to Per-bank Refresh different bank time		tpbR2pbR	90	ns	3
REFpb to Activate command to different bank		tpbR2act	7.5	ns	
Refresh Management Cycle time (All Banks)		tRFMab	280	ns	3
Refresh Management Cycle time (Per Bank)		tRFMpb	190	ns	3
Refresh Cycle Time (All Banks): Enhanced DVFSC is Enabled		tRFCab	300	ns	4
Refresh Cycle time (Per Bank): Enhanced DVFSC is Enabled		tRFCpb	150	ns	4
Per-bank Refresh to Per-bank Refresh different bank time: Enhanced DVFSC is Enabled		tpbR2pbR	100	ns	4
Refresh Management Cycle time (All Banks): Enhanced DVFSC is Enabled		tRFMab	300	ns	4
Refresh Management Cycle time (Per Bank): Enhanced DVFSC is Enabled		tRFMpb	190	ns	4

Note(s):

(1) Refresh for each channel is independent of the other channel in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.

(2) 1x refresh rate (tREFW=32 ms) is supported at all temperatures at or below 85 °C Tcase. If MR4 OP[4:0] indicates a refresh rate of greater than 1x is supported, tREFW can be extended.

(3) Applied when Enhanced DVFSC is Disabled.

(4) Applied when Enhanced DVFSC is Enabled.

4.3 Speed Grade

OPERATING MODE / SPEED GRADE				LPDDR5X-7500	LPDDR5X-8533	Unit
DVFSC[2]	Enhanced DVFSC[6]	WCK:CK Ratio[3]	Banks[4]	Maximum Data Rate[1,]		
Disabled	Disabled	4:1	BG	7500	8533	Mbps
Disabled	Disabled	4:1	16B	3200	3200	
Disabled	Disabled	2:1	BG	Not Supported		
Disabled	Disabled	2:1	16B	3200	3200	
Enabled	Disabled	4:1	BG	Not Supported		
Enabled	Disabled	4:1	16B	1600	1600	
Enabled	Disabled	2:1	BG	Not Supported		
Enabled	Disabled	2:1	16B	1600	1600	
Disabled	Enabled	4:1	BG	Not Supported		
Disabled	Enabled	4:1	16B	3200	3200	
Disabled	Enabled	2:1	BG	Not Supported		
Disabled	Enabled	2:1	16B	3200	3200	
Link ECC Feature support by DRAM				Required		

Note(s):

(1) Speed grades represent the maximum data rate capability of the device. Higher speed grade devices can be operated at lower data rates. Achieving maximum data rates requires appropriate latency settings.

(2) DVFSC is enabled/disabled in MR19 OP[1:0] and MR13 OP[7].

(3) WCK:CK ratio is set in MR18 OP[7].

(4) Bank organization (BG or 16B) is set in MR3 OP[4:3].

(5) The LPDDR5X SDRAM supports the data-rate of DVFSQ up to 3200Mbps. As DVFSQ is enabled without an ODT, signal integrity of the channel between the memory and the DRAM controller should be guaranteed in advance. Please contact the vendor for enabling DVFSQ Data Rate over 3200 Mbps.

(6) Enhanced DVFSC is enabled/disabled in MR19 OP[1:0] and MR13 OP[7].Refer to MR41 OP[2:1] for Enhanced DVFSC mode support.

5.0 AC & DC Operating Conditions

5.1 Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
VDD1 Supply Voltage relative to VSS	VDD1	-0.4	2.1	V	
VDD2H Supply Voltage relative to VSS	VDD2H	-0.4	1.4	V	
VDD2L Supply Voltage relative to VSS	VDD2L	-0.4	1.4	V	
VDDQ Supply Voltage relative to VSS	VDDQ	-0.4	1.4	V	
Voltage on Any Ball Except VDD1 relative to VSS	VIN, VOUT	-0.4	1.4	V	
Storage Temperature	TSTG	-55	125	°C	1

Note(s):

(1) Storage Temperature is the case surface temperature on the center/top side of the LPDDR5 device. For the measurement conditions, please refer to JESD51-2A

5.2 DC Operating Conditions

DRAM	Symbol		Low Freq Voltage Spec Freq: DC to 2 MHz				Z(f) Spec Freq: 2 MHz to 10MHz		Z(f) Spec Freq: 20 MHz		Notes
			Min	Typ	Max	Units	Zmax	Units	Zmax	Units	
Core 1 Power	VDD1		1.70	1.80	1.95	V	100	mΩ	170	mΩ	1,2,9
Core 2 Power / Input Buffer Power	VDD2H		1.01	1.05	1.12	V	40	mΩ	80	mΩ	1,2,9
	VDD2L	Single Core Power Rail (MR13 P[7]=1B)	1.01	1.05	1.12	V	120	mΩ	190	mΩ	1,2,9
		Dual Core Power Rail (MR13 P[7]=0B)	0.87	0.90	0.97	V		mΩ		mΩ	1,2,9
I/O Buffer Power	VDDQ	SPEC Range 1	0.47	0.50	0.57	V	40	mΩ	80	mΩ	2,3,6,9
		SPEC Range 2	0.27	0.30	0.37	V		mΩ		mΩ	2,4,9
		Allowable Range	0.27	N/A	0.57	V	N/A		N/A		5,6,7,8

Note(s):

(1) VDD1 uses significantly less current than VDD2H and VDD2L.

(2) DC to 2MHz voltage range includes all noise at DRAM ball, both DC and AC ripple fluctuations. This noise is included in the aperture mask defined by VdIVW. Refer to Figure(1). DC voltage range .

(3) SPEC Range 1 is intended for IO operation with both ODT enabled and disabled.

(4) SPEC Range 2 is intended for IO operation with ODT disabled.

(5) IO operation at VDDQ levels between outside SPEC Range 1 or SPEC Range 2 is allowed with ODT disabled.

(6) Allowable range is valid only when DVFSQ enabled.

(7) 100mV tolerance(-30mV/+70mV) is applied to VDDQ allowable ranges. Refer to Figure(2). VDDQ tolerance definition in allowable range.

(8) Vendors may support 0.6V VDDQ(typ) as an option. Because ZQ calibration is optimized at VDDQ=0.5V, the output drive strength. May not be guaranteed at VDDQ=0.6V. Refer to a vendor's data sheet.

(9) Z(f) is defined for all pins per voltage domain per channel. Z(f) does not include the DRAM package and silicon die.

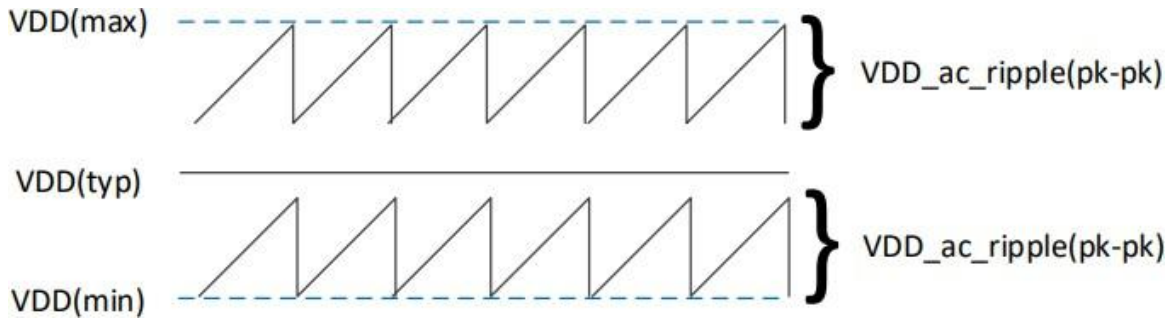


Figure (1). DC Voltage Range

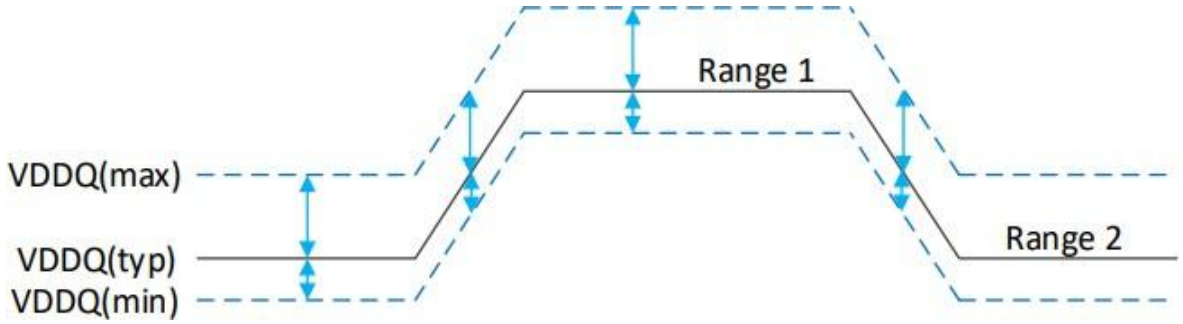


Figure (2). VDDQ Tolerance Definition in Allowable Range

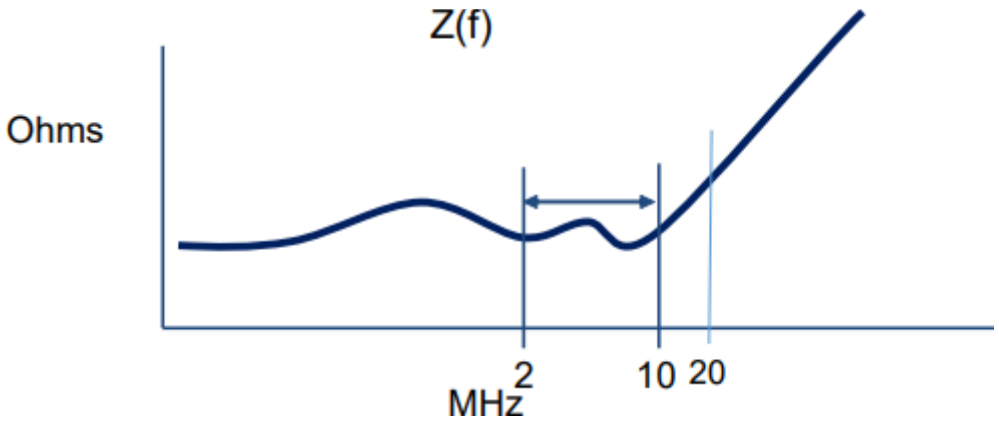


Figure (3). Zprofile Z(f) of the system at the DRAM package solder ball (without the DRAM component)

A simplified electrical system load model for Z(f) with the general frequency response is shown in Figure (4). The system resistance and inductance can be scaled to generalize the spec response to the DRAM pins.

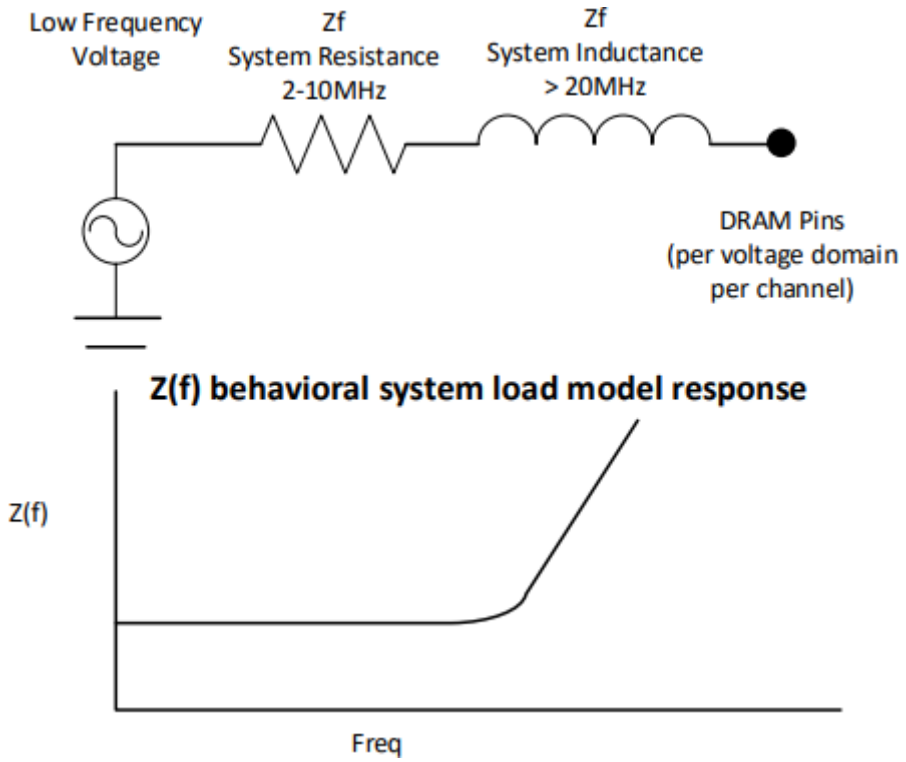


Figure (4). A simplified Z(f) system electrical model and frequency response of the behavioral PDN electrical load model without the DRAM component per voltage domain per channel.

5.3 Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input Leakage Current	I_L	-8	8	uA	1,2,3
CS Leakage Current	I_{LCS}	-16	16	uA	1,2,4,5

Note(s):

(1) For CK_t, CK_c, WCK_t, WCK_c, and CA. Any input 0V ≤ VIN ≤ VDDQ (All other pins not under test = 0 V).

(2) For CS and RESET_n. Any input 0V ≤VIN ≤ VDD2H (All other pins not under test = 0V).

(3) CA ODT is disabled for CA, CK ODT is disabled for CK_t and CK_c, and WCK ODT is disabled for WCK_t and WCK_c

(4) CS ODT is disabled for CS if optional CS ODT is supported.

(5) ILCS is applied when CS ODT is supported. If CS ODT is not supported, the input leakage current for CS shall meet IL.

5.4 Input / Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Units	Notes
Input/Output Leakage Current	I_{OZ}	-10	10	uA	1,2

Note(s):

(1) For DQ, RDQS_t, RDQS_c and DMI. Any I/O 0V ≤ VOUT ≤ VDDQ.

(2) I/Os status are disabled: High Impedance and ODT Off.

5.5 Operating Temperature Range

Parameter / Condition	Symbol	Min	Max	Units	Notes
Standard	$T_{oper\_standard}$	-25	85	℃	1,2

Note(s):

(1) Operating Temperature is the case surface temperature on the center-top side of the LPDDR5 device. For the measurement conditions, please refer to JESD51-2A.

(2) Either the device case temperature rating or the temperature sensor may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the TOPER rating that applies for the Standard Temperature Ranges. For example, TCASE may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

6.0 AC AND DC INPUT/OUTPUT MEASUREMENT LEVELS

6.1 1.05V High speed LVCMOS

6.1.1 Standard specifications

All voltages are referenced to ground except where noted.

6.1.2 Input Level for Reset_n

LPDDR5 uses CMOS with VDD2H Reset_n signaling to ensure stable LPDDR5 reset operation.

Item	Symbol	Min/Max	Value	Unit	Note
Reset_n ViH	ViH_RS	Min	0.8 x V_{DD2H}	V	
		Max	V_{DD2H} + 0.2	V	1
Reset_n ViL	ViL_RS	Min	-0.2	V	1
		Max	0.2 x V_{DD2H}	V	

Note(s):

(1) Refer to 6.1.4.

6.1.3 Input Level for CS

Parameter	Symbol	Min	Max	Unit	Note
Input High Level	V_{IH}	TBD	TBD	V	1
Input Low Level	V_{IL}	TBD	TBD	V	1

Note(s):

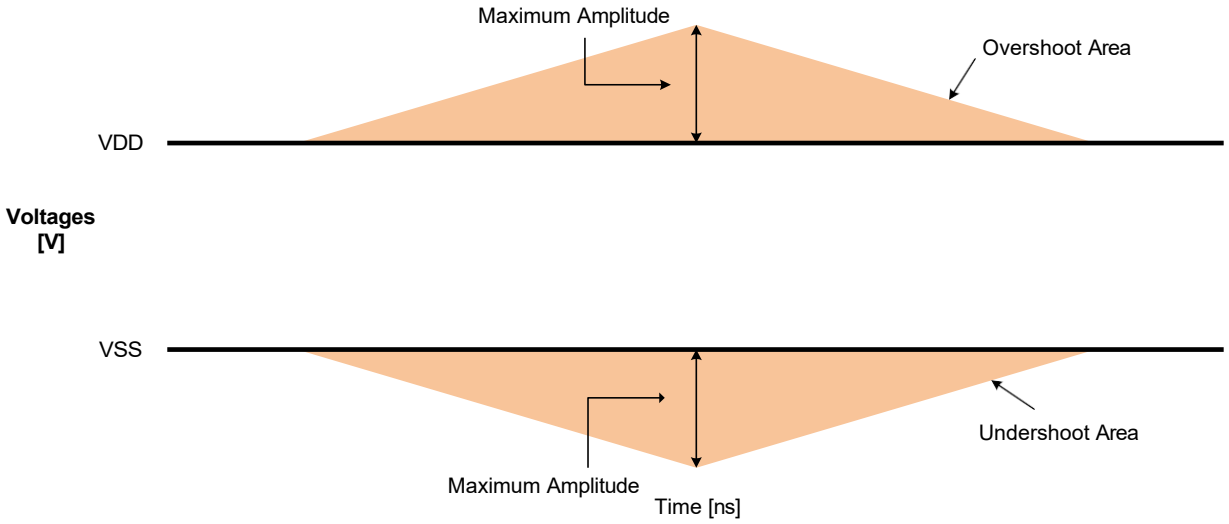
(1) Refer to 6.1.4.

6.1.4 AC Overshoot / Undershoot

Parameter	Specification
Maximum Peak Amplitude allowed for overshoot area	0.35V
Maximum Peak Amplitude allowed for undershoot area	0.35V
Maximum overshoot area above VDD2H/VDDQ	0.8V-ns
Maximum undershoot area above VSS	0.8V-ns

6.1.5 AC Overshoot / Undershoot for LVSTL

Parameter	Min/ Max	Data Rate				Units
		1600	3200	5500	6400	
Maximum Peak Amplitude allowed for overshoot area	Max	0.3	0.3	0.3	0.3	V
Maximum Peak Amplitude allowed for undershoot area	Max	0.3	0.3	0.3	0.3	V
Maximum overshoot area above VDD2H/VDDQ	Max	0.1	0.1	0.1	0.1	V-ns
Maximum undershoot area above VSS	Max	0.1	0.1	0.1	0.1	V-ns



Note(s):

(1) VDD is VDD2H for CS and RESET_n. VDD is VDDQ for CA[6:0], CK_t/c, DQ, DMI, RDQS_t, WCK_t/c.

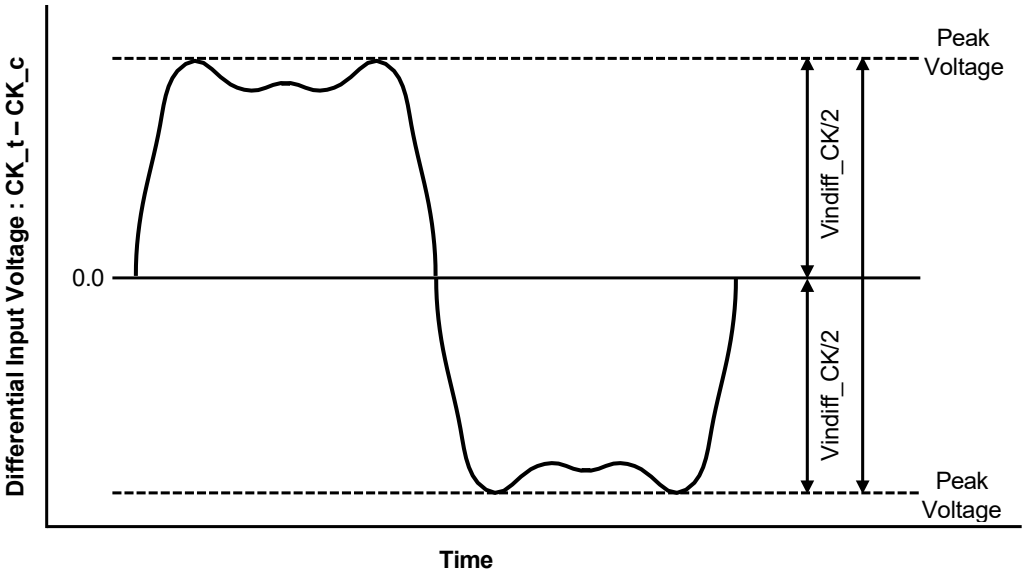
(2) Maximum peak amplitude values are referenced from actual VDD and VSS values.

(3) Maximum area values are referenced from maximum operating VDD and VSS values.

6.2 Differential Input Voltage

6.2.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.



Parameter	Symbol	Clock Rate										Unit	Note
		266MHz		533MHz		800MHz		937 MHz		1066MHz			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
CK Differential Input Voltage	Vindiff_CK	350	-	350	-	350	-	350	-	350	-	mV	1,2

Note(s):

(1) Refer to the latency table to match the clock rate to data rate.

(2) The peak voltage of Differential CK signals is calculated in a following equation.

Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)

Max Peak Voltage = Max(f(t))

Min Peak Voltage = Min(f(t))

f(t) = VCK_t - VCK_c

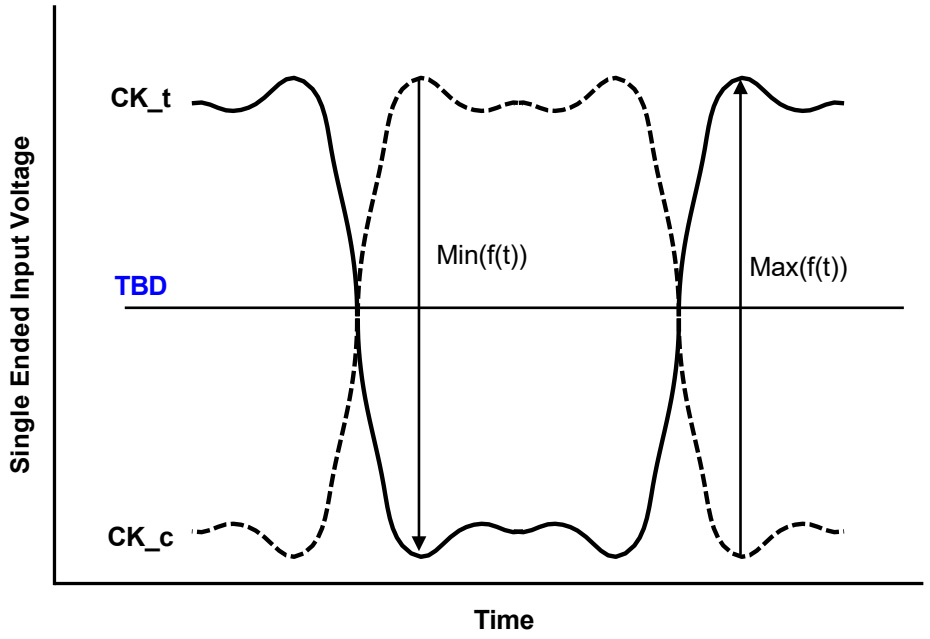
6.2.2 Peak Voltage Calculation Method

The peak voltage of Differential Clock signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VCK_t - VCK_c

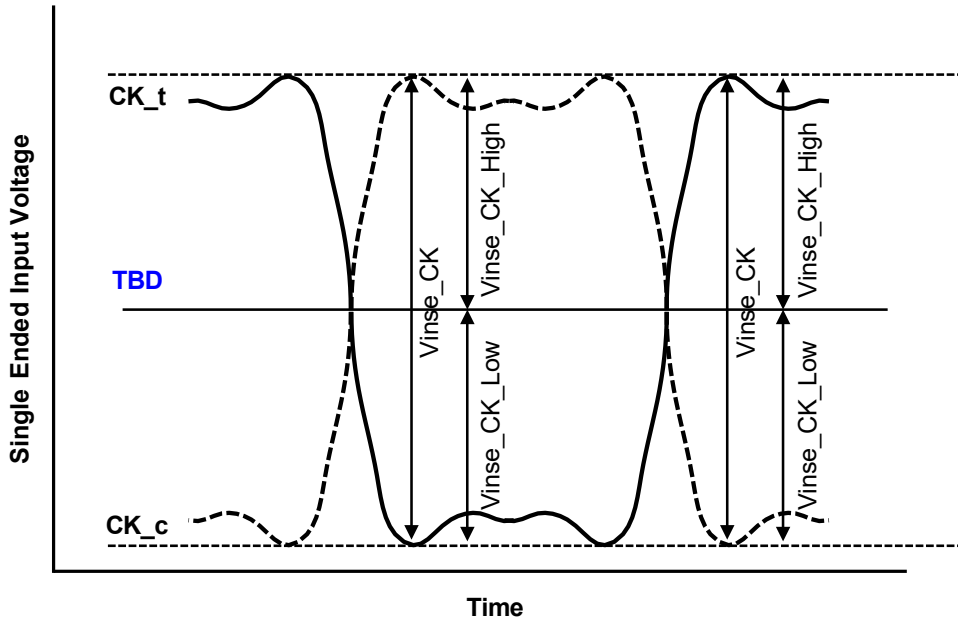


Note(s):

(1) TBD is LPDDR5 SDRAM internal setting value by Vref training.

6.2.3 Single ended Input Voltage for CK

The minimum input voltage needs to satisfy both Vinse_CK, Vinse_CK_High/Low specification at input receiver.



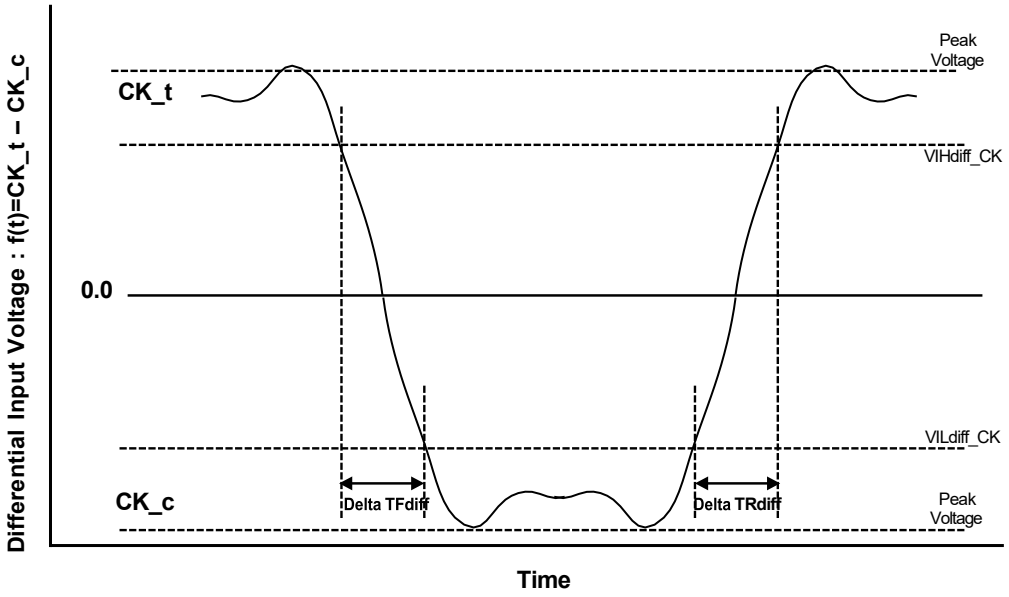
Note(s):

(1) TBD is LPDDR5 SDRAM internal setting value by Vref training.

Parameter	Symbol	Clock Rate										Unit
		266MHz		533MHz		800MHz		937MHz		1066MHz		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Single-ended input Voltage	Vinse_CK	175	-	175	-	175	-	175	-	175	-	mV
Clock Single-ended input Voltage High from TBD	Vinse_CK_High	87.5	-	87.5	-	87.5	-	87.5	-	87.5	-	mV
Clock Single-ended input Voltage Low from TBD	Vinse_CK_Low	87.5	-	87.5	-	87.5	-	87.5	-	87.5	-	mV

6.2.4 Differential Input Slew Rate Definition for CK

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in figure and the following Tables.



Note(s):

(1) Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.

(2) Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t - CK_c)	VILdiff_CK	VIHdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTFdiff

Differential Input Level for CK_t, CK_c

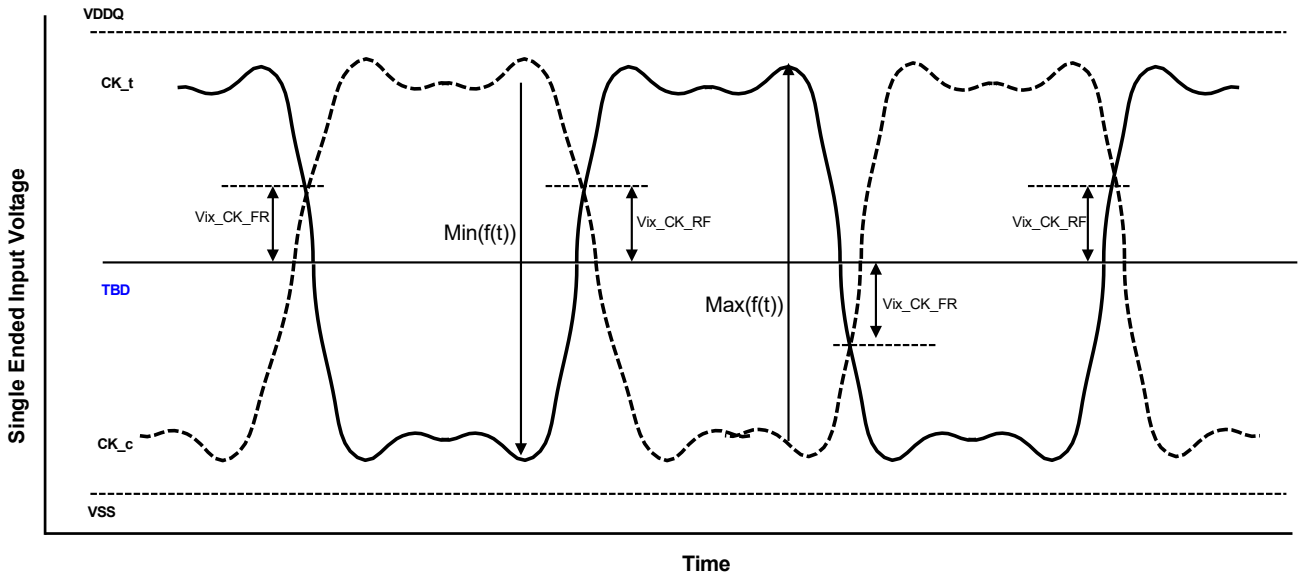
Parameter	Symbol	Clock Rate										Unit
		266MHz		533MHz		800MHz		937MHz		1066MHz		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential Input High	VIHdiff_CK	145	-	145	-	145	-	145	-	145	-	mV
Differential Input Low	VILdiff_CK	-	145	-	145	-	145	-	145	-	145	mV

Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	Clock Rate										Unit
		266MHz		533MHz		800MHz		937MHz		1066MHz		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	2	14	2	14	2	14	2	14	V/ns

6.2.5 Differential Input Cross Point Voltage for CK

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in the following Table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is TBD.



Note(s):

(1) The base level of Vix_CK_FR/RF is TBD that is LPDDR5 SDRAM internal setting value by Vref training.

Cross point voltage for differential input signals (Clock)

Parameter	Symbol	Clock Rate										Unit	Note
		266MHz		533MHz		800MHz		937MHz		1066MHz			
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Differential input crosspoint voltage ratio	Vix_CK _ratio	-	25	-	25	-	25	-	25	-	25	%	1,2

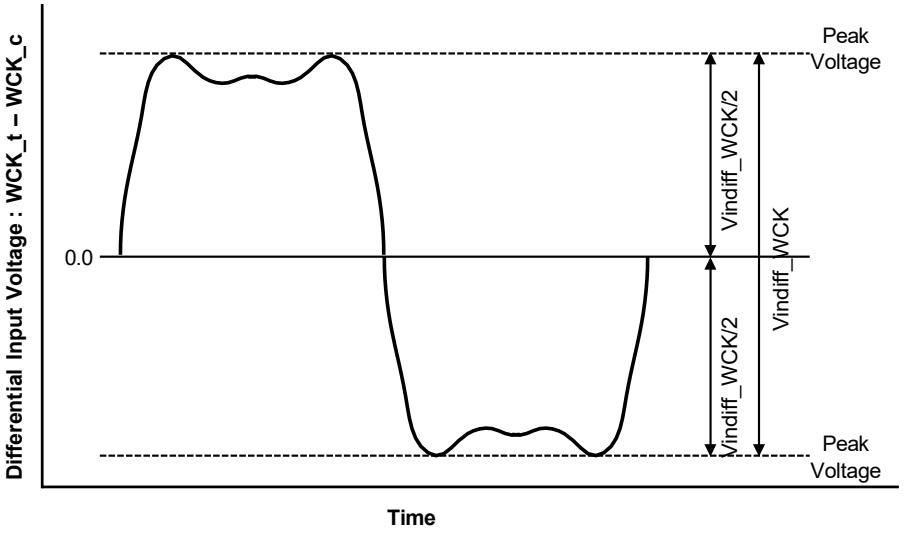
Note(s):

(1) Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|

(2)) Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))

6.3 Differential Input Voltage for WCK

The minimum input voltage needs to satisfy both Vindiff_WCK and Vindiff_WCK /2 specification at input receiver and their measurement period is 1tWCK. Vindiff_WCK is the peak to peak voltage centered on 0 volts differential and Vindiff_WCK /2 is max and min peak voltage from 0V



Parameter	Symbol	WCK Rate [MHz]								Unit	Note
		800		1066		1600		2133			
		Min	Max	Min	Max	Min	Max	Min	Max		
WCK Differential Input Voltage	Vindiff_WCK	300	-	300	-	300	-	280	-	mV	1,2

Parameter	Symbol	WCK Rate [MHz]								Unit	Note
		2750		3200		3750		4266.5			
		Min	Max	Min	Max	Min	Max	Min	Max		
WCK Differential Input Voltage	Vindiff_WCK	280	-	280	-	280	-	280	-	mV	1,2

Note(s):

(1) Refer to Read Latencies for Read Link ECC off case (DVFSC disabled) table to match the WCK rate to data rate.

(2) The peak voltage of Differential WCK signals is calculated in a following equation.

Vindiff_WCK = (Max Peak Voltage) - (Min Peak Voltage)

Max Peak Voltage = Max(f(t))

Min Peak Voltage = Min(f(t))

f(t) = VWCK_t - VWCK_c

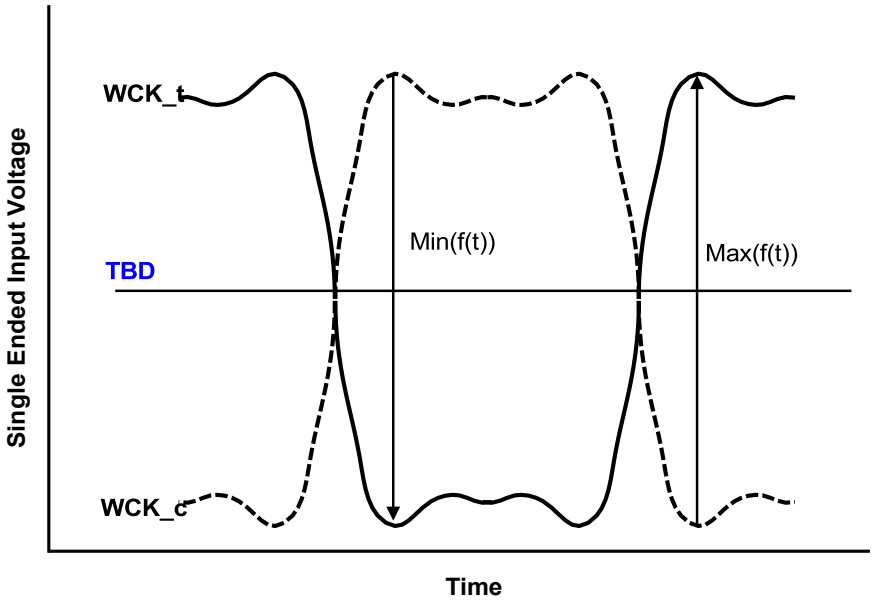
6.3.1 Peak Voltage Calculation Method

The peak voltage of Differential WCK signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))

VIL.DIFF.Peak Voltage = Min(f(t))

f(t) = VWCK_t - VWCK_c

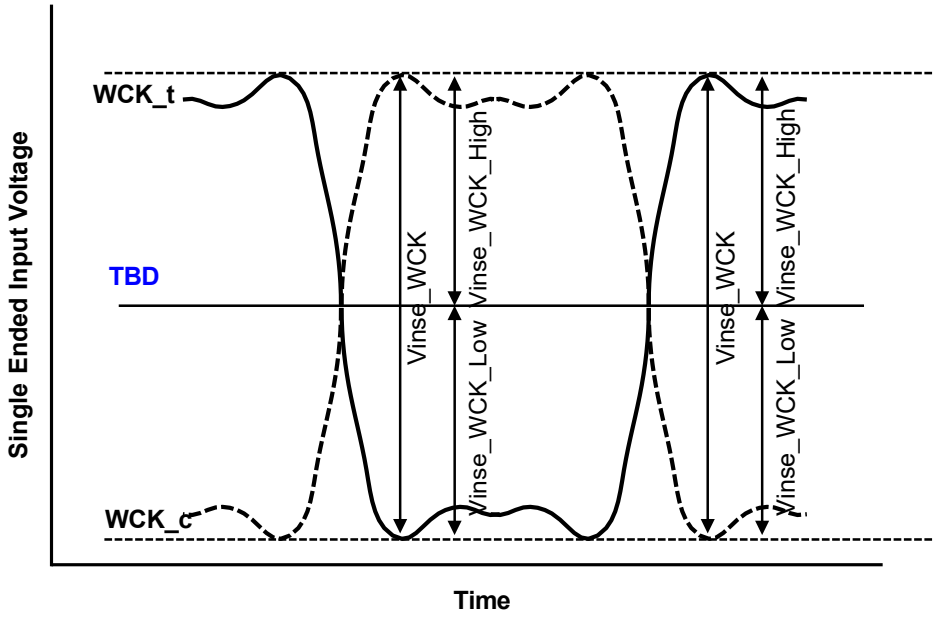


Note(s):

(1) TBD is LPDDR5 SDRAM internal setting value by Vref training.

6.3.2 Single ended Input Voltage for WCK

The minimum input voltage needs to satisfy both Vinse_WCK, Vinse_WCK_High/Low specification at input receiver.



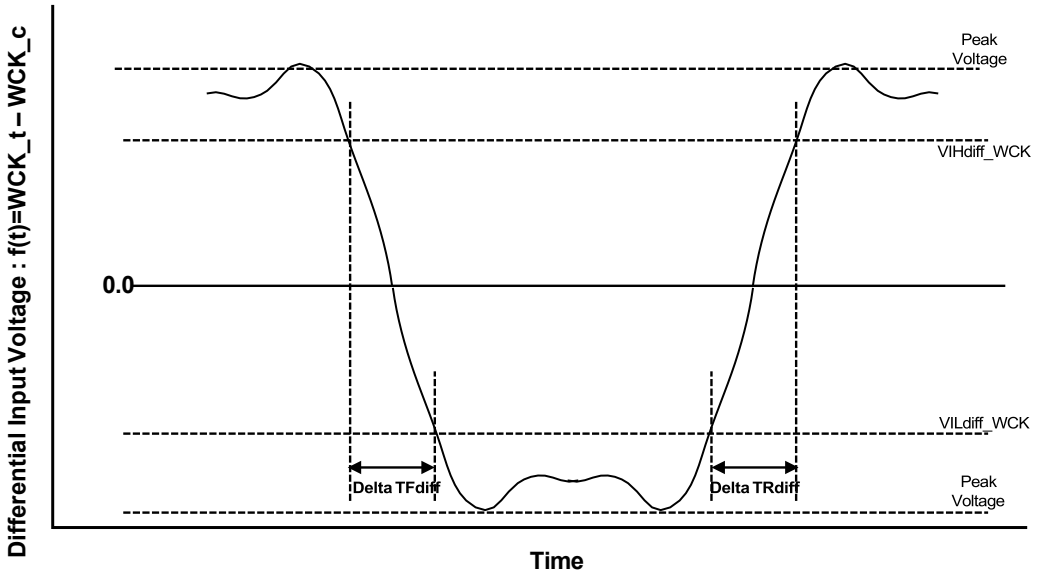
Note(s):

(1) TBD is LPDDR5 SDRAM internal setting value by Vref training.

Parameter	Symbol	WCK Rate [MHz]				Unit
		800/1066/1600		2133/2175/3200/3750/4266.5		
		Min	Max	Min	Max	
WCK Single-ended input Voltage	Vinse_WCK	150	-	140	-	mV
WCK Single-ended input Voltage High from TBD	Vinse_WCK_High	75	-	70	-	mV
WCK Single-ended input Voltage Low from TBD	Vinse_WCK_Low	75	-	70	-	mV

6.3.3 Differential Input Slew Rate Definition for WCK

Input slew rate for differential signals (WCK_t, WCK_c) are defined and measured as shown in figure and the following Tables.



Note(s):

(1) Differential signal rising edge from VILdiff_WCK to VIHdiff_WCK must be monotonic slope.

(2) Differential signal falling edge from VIHdiff_WCK to VILdiff_WCK must be monotonic slope.

Differential Input Slew Rate Definition for WCK_t, WCK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (WCK_t - WCK_c)	VILdiff_WCK	VIHdiff_WCK	|VILdiff_WCK - VIHdiff_WCK|/DeltaTRdiff
Differential input slew rate for falling edge (WCK_t - WCK_c)	VIHdiff_WCK	VILdiff_WCK	|VILdiff_WCK - VIHdiff_WCK|/DeltaTFdiff

Differential Input Level for WCK_t, WCK_c

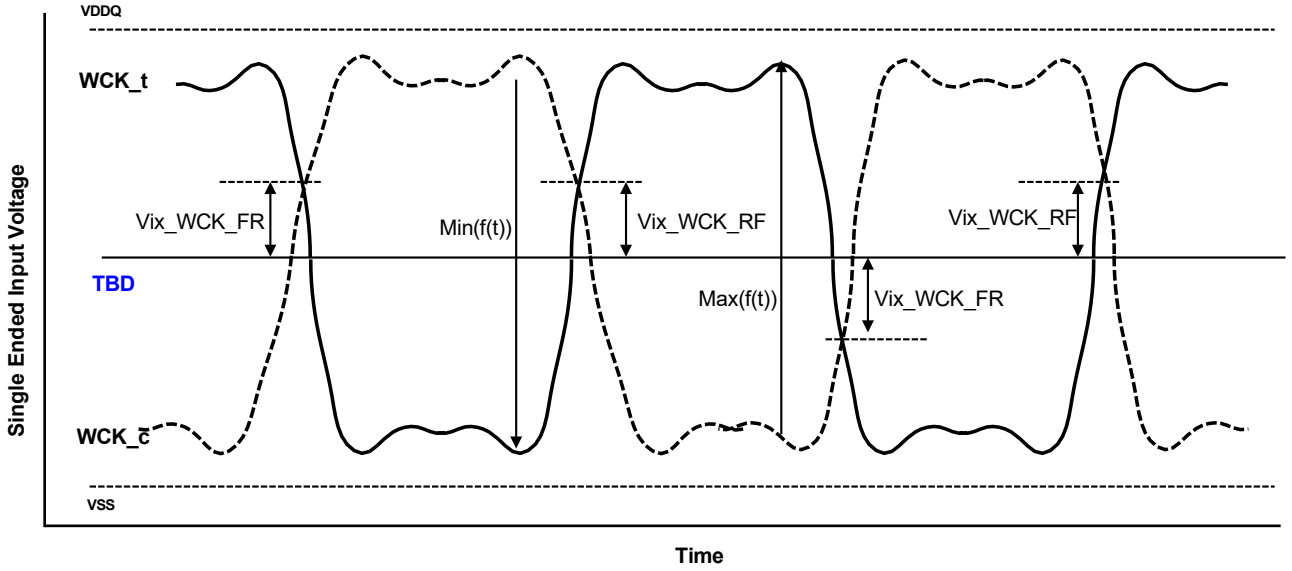
Parameter	Symbol	WCK Rate [MHz]				Unit
		800/1066/1600		2133/2175/3200/3750/4266.5		
		Min	Max	Min	Max	
Differential Input High	VIHdiff_WCK	120	-	100	-	mV
Differential Input Low	VILdiff_WCK	-	120	-	100	mV

Differential Input Slew Rate for WCK_t, WCK_c

Parameter	Symbol	WCK Rate [MHz]				Unit
		800/1066/16002133/2175/3200		3750/4266.5		
		Min	Max	Min	Max	
Differential Input Slew Rate for WCK	SRIdiff_WCK	2	14	3	14	mV

6.3.4 Differential Input Cross Point Voltage for WCK

The cross point voltage of differential input signals (WCK_t, WCK_c) must meet the requirements in the following Table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is TBD.



Note(s):

(1) The base level of Vix_WCK_FR/RF is TBD that is LPDDR5 SDRAM internal setting value by Vref training.

Cross point voltage for differential input signals (WCK)

Parameter	Symbol	WCK Rate [MHz]		Unit	Note
		800/1066/1600/2133/2750/3200/3750/4266.5			
		Min	Max		
WCK Differential input crosspoint voltage ratio	Vix_WCK _ratio	-	20	%	1,2

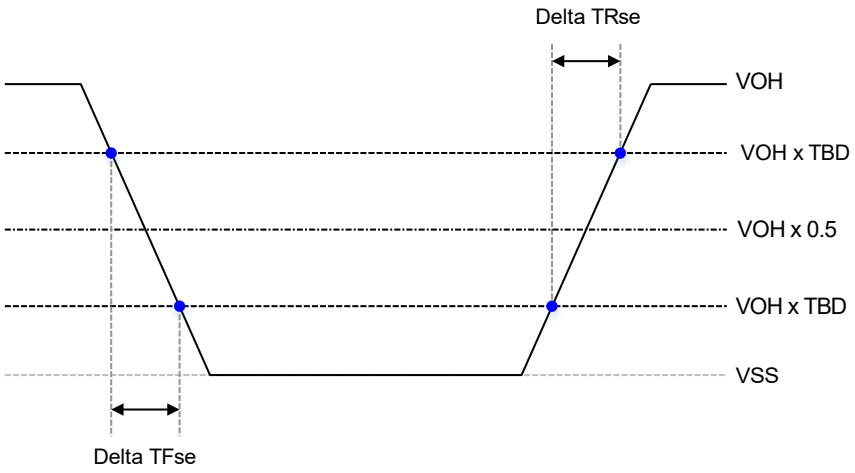
Note(s):

(1) Vix_WCK_Ratio is defined by this equation: Vix_WCK_Ratio = Vix_WCK_FR/|Min(f(t))|

(2) Vix_WCK_Ratio is defined by this equation: Vix_WCK_Ratio = Vix_WCK_RF/Max(f(t))

6.4 Output Slew Rate

6.4.1 Single Ended Output Slew Rate

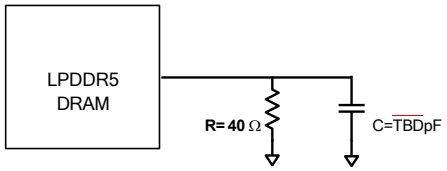


Parameter	Symbol	Value		Units
		Min	Max	
Single-ended Output Slew Rate	SRQse	TBD	TBD	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	TBD	TBD	-

Description: SR: Slew Rate ; Q: Query Output (like in DQ, which stands for Data-in, Query-Output) ; se: Single-ended Signals

Note(s):

(1) These values are measured with the following output reference load or guaranteed by design.



(2) The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process

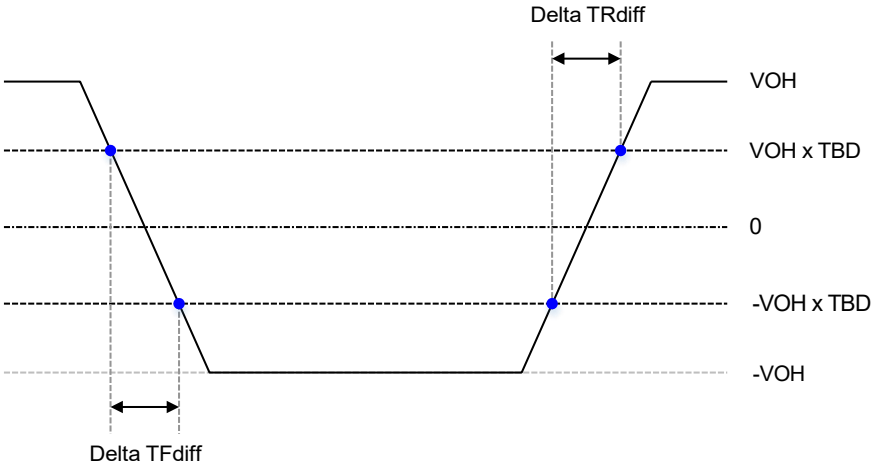
variation.

(3) The output slew rate for falling and rising edges is defined and measured between VOH x TBD and VOH x TBD.

(4) Slew rates are measured using a unit step signal which makes a full swing signal under average SSO conditions, with 50% of DQ signals per data byte switching. Because a high capacitance load reduces Voh(ac) at high frequency close to Fmax, the signal using PRBS data pattern may not achieve a full swing at such conditions.

(5) The parameters about Single-ended applies to RDQS_t and RDQS_c when either RDQS_t or RDQS_c is disabled.

6.4.2 Differential Output Slew Rate

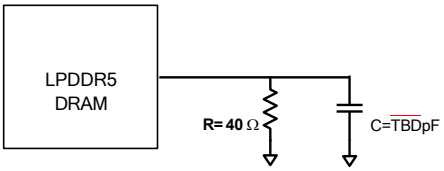


Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate	SRQdiff	TBD	TBD	V/ns

Description: SR: Slew Rate ; Q: Query Output (like in DQ, which stands for Data-in, Query-Output) ; diff: Differential Signals

Note(s):

(1) These values are measured with the following output reference load or guaranteed by design.



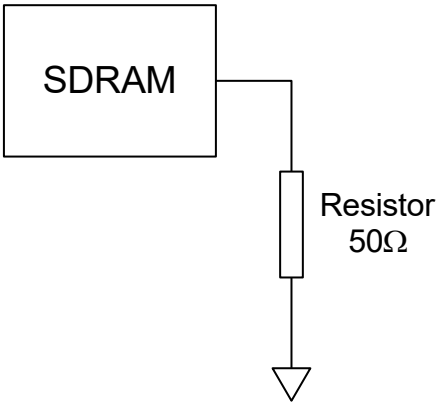
(2) The output slew rate for falling and rising edges is defined and measured between VOH x TBD and VOH x TBD.

(3) Slew rates are measured using a unit step signal which makes a full swing signal under average SSO conditions, with 50% of DQ signals per data byte switching. Because a high capacitance load reduces Voh(ac) at high frequency close to Fmax, the signal using PRBS data pattern may not achieve a full swing at such conditions.

6.5 Driver Output Timing Reference load

These "Timing Reference Loads" are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Driver Output Reference Load for Timing

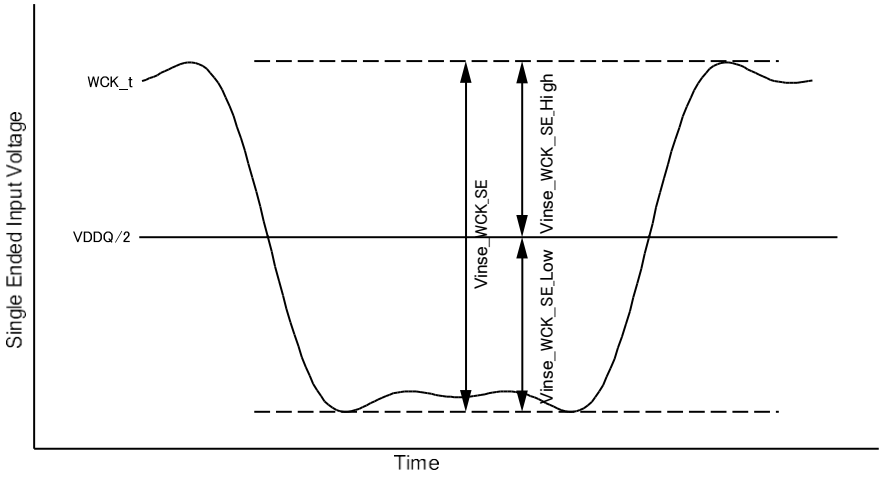


6.6 Single Ended WCK

6.6.1 Single Ended WCK input definitions

The minimum input voltage need to satisfy both Vinse_WCK_SE_High and Vinse_WCK_SE_Low specification at input receiver and their measurement period is 1tWCK. Vinse_WCK_SE is the peak to peak voltage centered on VDDQ/2 and Vinse_WCK_SE_High and Vinse_WCK_SE_Low is max and min peak voltage from VDDQ/2.

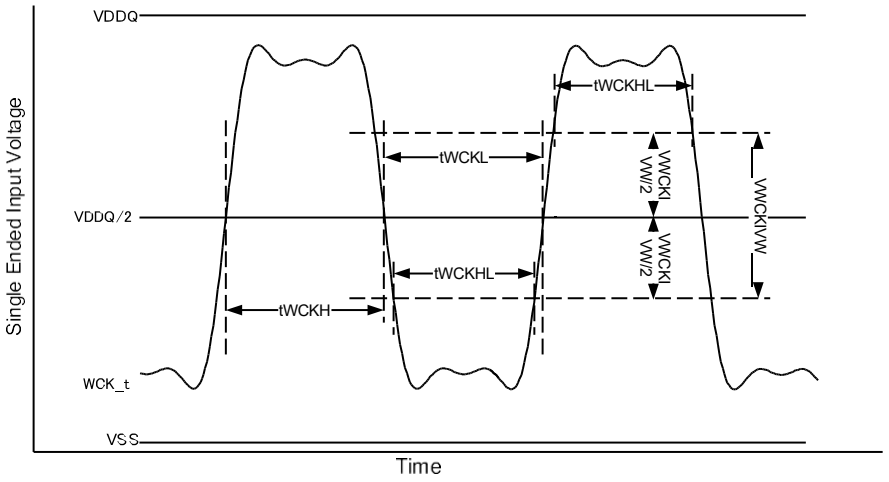
Single Ended Mode WCK input Voltage



6.6.2 Single Ended Mode WCK Pulse Definitions

Single Ended Mode WCK pulse definitions are defined shown below

Single Ended Mode WCK pulse



Parameter	Symbol	Min/ Max	WCK Frequency	Unit	Note
			800MHz		
WCK Single ended input voltage	Vinse_WCK_SE	Min	220	mV	
WCK Single Ended Input Voltage High	Vinse_WCK_SE _High	Min	110	mV	
WCK Single Ended Input Voltage Low	Vinse_WCK_SE _low	Min	110	mV	
WCK single ended timing window	VWCKIVW	Min	180	mV	
Clock Single Ended WCK Pulse	tWCKHL	Min	0.23	tWCK (avg)	
WCK single ended Slew Rate	SRIWCKSE	Min	1	V/ns	1
		Max	7	V/ns	

Note(s):

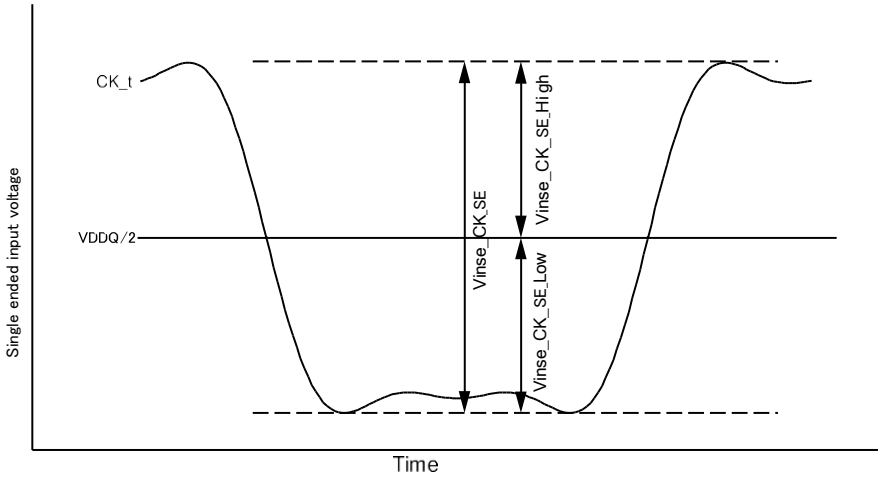
(1) Single ended slew rate is measured at VDDQ/2 - VWCKIVW/2 and VDDQ/2 + VWCKIVW/2

6.7 Single Ended CK

6.7.1 Single Ended CK input definitions

The minimum input voltage needs to satisfy both Vinse_CK_SE_High and Vinse_CK_SE_Low specification at input receiver and their measurement period is 1tCK. Vinse_CK_SE is the peak to peak voltage centered on VDDQ/2 and Vinse_CK_SE_High and Vinse_CK_SE_Low is max and min peak voltage from VDDQ/2.

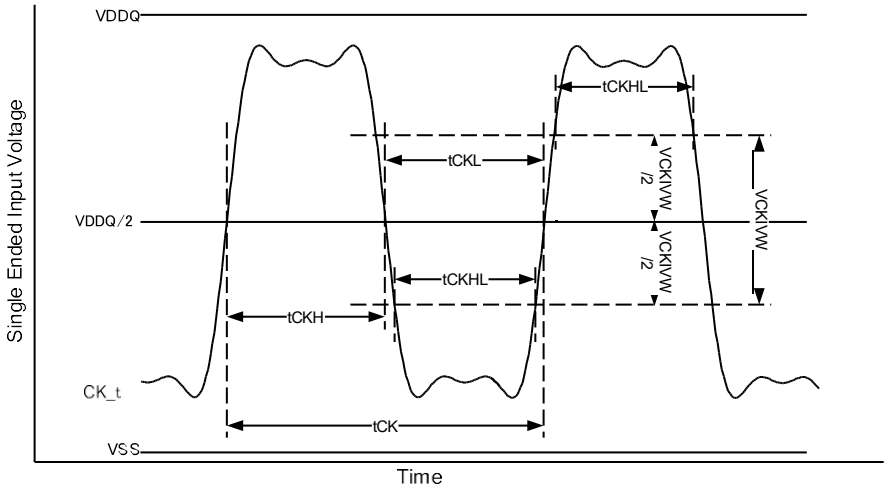
Single Ended Mode CK input Voltage



6.7.2 Single Ended Mode CK Pulse Definitions

Single Ended Mode CK pulse definitions are defined as shown in the following Table.

Single Ended Mode CK pulse



Parameter	Symbol	Min/ Max	CK Frequency	Unit	Note
			400MHz		
CK Single ended input voltage	Vinse_CK_SE	Min	220	mV	
CK Single Ended Input Voltage High	Vinse_CK_SE_High	Min	110	mV	
CK Single Ended Input Voltage Low	Vinse_CK_SE_low	Min	110	mV	
CK single ended timing window	VCKIVW	min	190	mV	
Clock Single Ended CK Pulse	tCKHL	Min	0.26	tCK(avg)	
CK single ended Slew Rate	SRICKSE	Min	1	V/ns	1
		Max	7		

Note(s):

(1) Single ended slew rate is measured at VDDQ/2 - VCKIVW/2 and VDDQ/2 + VCKIVW/2

6.8 Pull Up/Pull Down Driver Characteristics and Calibration

All output pins (DQ, DMI, RDQS_t and RDQS_c) driver characteristics and calibration are defined following.

Pull-down Driver Characteristics, with ZQ Calibration

R_{ONPD},nom	Resistor	Min	Nom	Max	Unit
40 Ohm	R_{ON40PD}	0.9	1	1.1	RZQ/6
48 Ohm	R_{ON48PD}	0.9	1	1.1	RZQ/5
60 Ohm	R_{ON60PD}	0.9	1	1.1	RZQ/4
80 Ohm	R_{ON80PD}	0.9	1	1.1	RZQ/3
120 Ohm	$R_{ON120PD}$	0.9	1	1.1	RZQ/2
240 Ohm	$R_{ON240PD}$	0.9	1	1.1	RZQ/1

Note(s):

(1) All value are after ZQ Calibration. Without ZQ Calibration RONPD values are ± 30%.

(2) RONPD limits are defined at same voltage and temperature as at the time ZQ calibration was done.

Pull-up Characteristics, with ZQ Calibration

VOH_{PU},nom	VOH,nom(mV)	Min	Nom	Max	Unit
V_{DDQ}*0.5	250	0.9	1	1.1	VOH, nom

Note(s):

(1) All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are ± 30%.

(2) VOH,nom (mV) values are based on a nominal VDDQ = 0.5V, VDD2H=1.05V.

(3) VOHPU limits are defined at same voltage and temperature as at the time ZQ calibration was done.

(4) VOHPU limits are defined for load termination matching the SOC ODT setting (in MR17 OP[2:0]) selected at the time ZQ calibration was done. If the selected SOC ODT setting MR17 OP[2:0]=000B, then the VOHPU limits are not defined.

(5) VOHPU limits are defined as DC levels when all DQ drivers are driving high.

(6) Assumption of SOC ODT is typical for VOHPU,nom definition.

Valid Calibration Points

VOH_{PU},nom	ODT Value					
	240	120	80	60	48	40
V_{DDQ}*0.5	VALID	VALID	VALID	VALID	VALID	VALID

Note(s):

(1) Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.

Un-terminated Pull Up Characteristics

R_{ONUNPU},nom	Resistor	Min	Nom	Max	Unit
40 Ohm	$R_{ON40UNPU}$	0.7	1	1.3	RZQ/6
48 Ohm	$R_{ON48UNPU}$	0.7	1	1.3	RZQ/5
60 Ohm	$R_{ON60UNPU}$	0.7	1	1.3	RZQ/4
80 Ohm	$R_{ON80UNPU}$	0.7	1	1.3	RZQ/3
120 Ohm	$R_{ON120UNPU}$	0.7	1	1.3	RZQ/2
240 Ohm	$R_{ON240UNPU}$	0.7	1	1.3	RZQ/1

Pull-down Driver Characteristics in Enhanced DVFSC Mode

R_{ONPDED},nom	Resistor	Min	Nom	Max	Unit
40 Ohm	$R_{ON40PDED}$	0.45	1.0	1.75	RZQ/6
48 Ohm	$R_{ON48PDED}$	0.45	1.0	1.75	RZQ/5
60 Ohm	$R_{ON60PDED}$	0.45	1.0	1.75	RZQ/4
80 Ohm	$R_{ON80PDED}$	0.45	1.0	1.75	RZQ/3
120 Ohm	$R_{ON120PDED}$	0.45	1.0	1.75	RZQ/2
240 Ohm	$R_{ON240PDED}$	0.45	1.0	1.75	RZQ/1

Un-terminated Pull Up Characteristics in Enhanced DVFSC mode

$R_{ONUNPUED}$,nom	Resistor	Min	Nom	Max	Unit
40 Ohm	$R_{ON40UNPUED}$	0.45	1.0	1.75	RZQ/6
48 Ohm	$R_{ON48UNPUED}$	0.45	1.0	1.75	RZQ/5
60 Ohm	$R_{ON60UNPUED}$	0.45	1.0	1.75	RZQ/4
80 Ohm	$R_{ON80UNPUED}$	0.45	1.0	1.75	RZQ/3
120 Ohm	$R_{ON120UNPUED}$	0.45	1.0	1.75	RZQ/2
240 Ohm	$R_{ON240UNPUED}$	0.45	1.0	1.75	RZQ/1

6.9 Output Driver and Termination Resistance Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Worst Case Output Driver and Termination Resistance

Resistor	Definition Point	Min	Max	Unit	Notes
$R_{ON}PD$	0.5 x VDDQ	RonPD(nom) x(0.90-($dR_{on}dT$(max) x |ΔT|) -(dR_{on}(max)dV2 x|ΔV2|) -(dR_{on}(max)dVQ x|ΔVQ|))	RonPD(nom)x(1.10+(dR_{on}(max)dT x |ΔT|) +(dR_{on}(max)dV2 x|ΔV2|) +(dR_{on}(max)dVQ x|ΔVQ|))	ohm	1,2,3
R_{TT}	0.5 x VDDQ	R_{TT} (nom) x(0.90-(dR_{on}(max)dT x |ΔT|) -(dR_{on}(max)dV2 x|ΔV2|) -(dR_{on}(max)dVQ x|ΔVQ|))	R_{TT} (nom) x(1.10+(dR_{on}(max)dT x |ΔT|) +(dR_{on}(max)dV2 x|ΔV2|) +(dR_{on}(max)dVQ x|ΔVQ|))	ohm	1,2,3
R_{ON}UNPU	0.5 x VDDQ	RonUNPU (nom) x(0.70-(dR_{on}UNdT(max) x |ΔT|) -(dR_{on}(max) UNdV2 x|ΔV2|) -(dR_{on}(max) UNdVQ x|ΔVQ|))	RonUNPU (nom)x(1.30+(dR_{on}(max) UNdT x |ΔT|) +(dR_{on}(max) UNdV2 x|ΔV2|) +(dR_{on}(max) UNdVQ x|ΔVQ|))	ohm	2,3
R_{TT}CS	0.5 x VDDQ	R_{TT}CS (nom) x(0.90-(dR_{on}(max)dT x |ΔT|) -(dR_{on}(max)dV2 x|ΔV2|) -(dR_{on}(max)dVQ x|ΔV2|))	R_{TT} CS (nom) x(1.10+(dR_{on}(max)dT x |ΔT|) +(dR_{on}(max)dV2 x|ΔV2|) +(dR_{on}(max)dVQ x|ΔV2|))	ohm	1,2,3
R_{ON}PDED	0.5 x VDDQ	RonPDED(nom) x(0.45-(dR_{on}PDEDdT(max) x |ΔT|) -(dR_{on}(max)PDEDdV2 x|ΔV2|) -(dR_{on}(max)PDEDdVQ x|ΔVQ|))	RonPDED(nom) x(1.75-(dR_{on}PDEDdT(max) x |ΔT|) -(dR_{on}(max)PDEDdV2 x|ΔV2|) -(dR_{on}(max)PDEDdVQ x|ΔVQ|))	ohm	1,2,3,4
R_{TT}ED	0.5 x VDDQ	R_{TT}ED(nom) x(0.45-(dR_{on}PDEDdT(max) x |ΔT|) -(dR_{on}(max)PDEDdV2 x|ΔV2|) -(dR_{on}(max)PDEDdVQ x|ΔVQ|))	R_{TT}ED(nom) x(1.75-(dR_{on}PDEDdT(max) x |ΔT|) -(dR_{on}(max)PDEDdV2 x|ΔV2|) -(dR_{on}(max)PDEDdVQ x|ΔVQ|))	ohm	1,2,3,4
R_{ON}UNPUED	0.5 x VDDQ	RonUNPUED (nom) x(0.45-(dR_{on}UNEDdT(max) x |ΔT|) -(dR_{on}(max) UNEDdV2 x|ΔV2|) -(dR_{on}(max) UNEDdVQ x|ΔVQ|))	RonUNPUED (nom) x(1.75-(dR_{on}UNEDdT(max) x |ΔT|) -(dR_{on}(max) UNEDdV2 x|ΔV2|) -(dR_{on}(max) UNEDdVQ x|ΔVQ|))	ohm	1,2,3,4

Note(s):

(1) ΔT = T - T(@ Calibration), ΔV2 = VDD2H - VDD2H(@ Calibration), ΔVQ = VDDQ - VDDQ(@ Calibration)

(2)) dRONdT, dRONdV2, dRONdVQ, dRTTdV2, dRTTdVQ, dRTTdT, dRONUNdT, dRONUNdV2 and dRONUNdVQ are not subject to production test but are verified by design and characterization.

(3) VDD1, VDD2H, VDD2HQ and VDDQ must be nominal during measurement.

(4) RONPDED, RTTED and RONUNPUED apply at Enhanced DVFSC mode is enabled.

Worst Case Output high voltage

Voltage	Min	Max	Unit	Notes
V_{OHPU}	V_{OHPU} (nom) x(0.90-(dVOH(max)dT x |ΔT|)-(dVOH(max)dV2 x|ΔV2|)-(dVOH(max)dVQ x|ΔVQ|))	V_{OHPU} (nom) x(1.10+(dVOH(max)dT x |ΔT|)+(dVOH(max)dV2 x|ΔV2|)+(dVOH(max)dVQ x|ΔVQ|))	V	1,2,3,4

Note(s):

(1) ΔT = T - T(@ Calibration), ΔV2 = VDD2H – VDD2H(@ Calibration), ΔVQ = VDDQ – VDDQ(@ Calibration)

(2) dVOHdT, dVOHdV2 and dVOHdVQ are not subject to production test but are verified by design and characterization.

(3) Refer to Pull Up/Pull Down Driver Characteristics for VOHPU

(4) VDD1, VDD2H, VDD2HQ and VDDQ must be nominal during measurement.

Output Driver and Termination Resistance Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit	Notes
$dR_{ON}dT$	R_{ON} Temperature Sensitivity	0.00	0.75	%/°C	
$dR_{ON}dV2$	R_{ON} VDD2H Voltage Sensitivity	0.00	0.50	%/mV	
$dR_{ON}dVQ$	R_{ON} VDDQ Voltage Sensitivity	0.00	0.20	%/mV	
dVOHdT	VOH Temperature Sensitivity	0.00	0.75	%/°C	
dVOHdV2	VOH VDD2H Voltage Sensitivity	0.00	0.35	%/mV	
dVOHdVQ	VOH VDDQ Voltage Sensitivity	0.00	0.35	%/mV	
$dR_{TT}dT$	R_{TT} Temperature Sensitivity	0.00	0.75	%/°C	
$dR_{TT}dV2$	R_{TT} VDD2H Voltage Sensitivity	0.00	0.50	%/mV	
$dR_{TT}dVQ$	R_{TT} VDDQ Voltage Sensitivity	0.00	0.20	%/mV	
dRONUNdT	Un-terminated RON Temperature Sensitivity	0.00	0.75	%/°C	
dRONUNdV2	Un-terminated RON VDD2H Voltage Sensitivity	0.00	0.75	%/mV	
dRONUNdVQ	Un-terminated RON VDDQ Voltage Sensitivity	0.00	0.75	%/mV	
dRonPDEDdT	R_{ON} Temperature Sensitivity	0.00	0.75	%/°C	1
dRonPDEDdV2	R_{ON} VDD2L Voltage Sensitivity	0.00	0.60	%/mV	1
dRonPDEDdVQ	R_{ON} VDDQ Voltage Sensitivity	0.00	0.20	%/mV	1
dRonUNEDdT	Un-terminated R_{ON} Temperature Sensitivity	0.00	0.75	%/°C	1
dRonUNEDdV2	Un-terminated R_{ON} VDD2L Voltage Sensitivity	0.00	0.75	%/mV	1
dRonUNEDdVQ	Un-terminated R_{ON} VDDQ Voltage Sensitivity	0.00	0.75	%/mV	1

Note(s):

(1) These parameters apply at Enhanced DVFSC mode is enabled.

7.0 Input / Output Capacitance

Parameter	Symbol		LPDDR5 6400	LPDDR5X 7500/8533	Units	Notes
Input Capacitance, CK_t and CK_c	CCK	Min	0.30	0.30	pF	1,2
		Max	0.80	0.80	pF	1,2
Input Capacitance delta, CK_t and CK_c	CDCK	Min	0.00	0.00	pF	1,2,3
		Max	0.09	0.09	pF	1,2,3
Input Capacitance, WCK_t and WCK_c	CWCK	Min	0.30	0.30	pF	1,2
		Max	0.90	0.80	pF	1,2
Input Capacitance delta, WCK_t and WCK_c	CDWCK	Min	0.00	0.00	pF	1,2,4
		Max	0.09	0.09	pF	1,2,4
Input Capacitance, All other input-only pins	CI	Min	0.30	0.30	pF	1,2,5
		Max	0.80	0.80	pF	1,2,5
Input Capacitance delta, All other input-only pins	CDI	Min	-0.10	-0.10	pF	1,2,6
		Max	0.10	0.10	pF	1,2,6
Input/output Capacitance, DQ and DMI	CIO	Min	0.30	0.30	pF	1,2,7
		Max	0.90	0.80	pF	1,2,7
Inputt/output Capacitance delta, DQ and DMI	CDIO	Min	-0.10	-0.10	pF	1,2,9
		Max	0.10	0.10	pF	1,2,9
Output Capacitance, RDQS_t and RDQS_c	COO	Min	0.30	0.30	pF	1,2
		Max	0.90	0.80	pF	1,2
Output Capacitance delta, RDQS_t and RDQS_c	CDOO	Min	0.00	0.00	pF	1,2,8
		Max	0.10	0.10	pF	1,2,8
Input/output Capacitance, ZQ pin	CZQ	Min	0.00	0.00	pF	1,2
		Max	5.00	5.00	pF	1,2

Note(s):

(1) This parameter applies to die device, including IO capacitance, RDL if needed (does not include package capacitance such as bond wire).

(2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS applied and all other pins floating).

(3) Absolute value of CCK_t - CCK_c

(4) Absolute value of CWCK_t - CWCK_c

(5) CI applies to CS, CA0~CA6

(6) CDI = CI – Average (CInputn, CCK_t, CCK_c).

(7) DMI loading matches DQ.

(8) Absolute value of CRDQS_t - CRDQS_c.

(9) CDIO = CIO – Average (CDQn, CDMI) in byte-lane.

8.0 IDD Specification Parameters and Conditions

8.1 IDD Specifications Parameters

Parameter / Condition	Symbol	Power Supply	Note
Operating one bank active-Precharge current: tCK = tCKmin; tRC = tRCmin; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD0_1$	VDD1	9
	$IDD0_{2H}$	VDD2H	9
	$IDD0_{2L}$	VDD2L	9
	$IDD0_Q$	VDDQ	3
Idle power-down standby current: tCK = tCKmin; Power-down entry command is issued CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD2P_1$	VDD1	
	$IDD2P_{2H}$	VDD2H	
	$IDD2P_{2L}$	VDD2L	
	$IDD2P_Q$	VDDQ	3
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD2PS_1$	VDD1	
	$IDD2PS_{2H}$	VDD2H	
	$IDD2PS_{2L}$	VDD2L	
	$IDD2PS_Q$	VDDQ	3
Idle non power-down standby current: tCK = tCKmin; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD2N_1$	VDD1	
	$IDD2N_{2H}$	VDD2H	
	$IDD2N_{2L}$	VDD2L	
	$IDD2N_Q$	VDDQ	3
Idle non power-down standby current with clock stopped: CK_t=LOW; CK_c=HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD2NS_1$	VDD1	
	$IDD2NS_{2H}$	VDD2H	
	$IDD2NS_{2L}$	VDD2L	
	$IDD2NS_Q$	VDDQ	3
Active power-down standby current: tCK = tCKmin; CS is LOW; One bank is active; Power-down entry command is issued CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable	$IDD3P_1$	VDD1	9
	$IDD3P_{2H}$	VDD2H	9
	$IDD3P_{2L}$	VDD2L	9
	$IDD3P_Q$	VDDQ	3

Parameter / Condition	Symbol	Power Supply	Note
Active power-down standby current with clock stop: Power-down entry command is issued CK_t=LOW, CK_c=HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	$IDD3PS_1$	VDD1	9
	$IDD3PS_{2H}$	VDD2H	9
	$IDD3PS_{2L}$	VDD2L	8, 9
	$IDD3PS_Q$	VDDQ	4
Active non-power-down standby current: tCK = tCKmin; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	$IDD3N_1$	VDD1	9
	$IDD3N_{2H}$	VDD2H	9
	$IDD3N_{2L}$	VDD2L	8, 9
	$IDD3N_Q$	VDDQ	4
Operating burst READ current @ BG Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; **One bank in each bank group 1 and 2 is active;** BL = 16 or 32 ; RL = RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_1$	VDD1	
	$IDD4R_{2H}$	VDD2H	
	$IDD4R_{2L}$	VDD2L	8
	$IDD4R_Q$	VDDQ	5
Operating burst READ current @ 8/16Bank Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; **One bank is active;** BL = 16 or 32 @ 16bank mode, BL=32 @ 8bank mode; RL = RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_1$	VDD1	
	$IDD4R_{2H}$	VDD2H	
	$IDD4R_{2L}$	VDD2L	8
	$IDD4R_Q$	VDDQ	5

Parameter / Condition	Symbol	Power Supply	Note
Operating burst READ current @ 8/16Bank Mode with DVFSC or E-DVFSC tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; **One bank is active;** BL = 16 or 32 @ 16bank mode, BL=32 @ 8bank mode; RL = RLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled **DVFSC or E-DVFSC mode is enabled**	$IDD4R_{DVFSC1}$	VDD1	11
	$IDD4R_{DVFSC2H}$	VDD2H	11
	$IDD4R_{DVFSC2L}$	VDD2L	8,11,12
	$IDD4R_{DVFSCQ}$	VDDQ	5,11
Operating burst WRITE current @ BG Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; **One bank in each bank group 1 and 2 is active;** BL = 16 or 32 ; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer RDQS_t is stable (if Link ECC is enabled) ODT disabled	$IDD4W_1$	VDD1	
	$IDD4W_{2H}$	VDD2H	
	$IDD4W_{2L}$	VDD2L	8
	$IDD4W_Q$	VDDQ	4
Operating burst WRITE current @ 8/16Bank Mode tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; **One bank is active;** BL = 16 or 32 @ 16bank mode, BL=32 @ 8bank mode ; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer RDQS_t is stable (if Link ECC is enabled) ODT disabled	$IDD4W_1$	VDD1	
	$IDD4W_{2H}$	VDD2H	
	$IDD4W_{2L}$	VDD2L	8
	$IDD4W_Q$	VDDQ	4
Operating burst WRITE current @ 8/16Bank Mode with DVFSC or E-DVFSC tCK = tCKmin; tWCK=tWCKmin; CS is LOW between valid commands; **One bank is active;** BL = 16 or 32 @ 16bank mode, BL=32 @ 8bank mode; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled **DVFSC or E-DVFSC mode is enabled**	$IDD4W_{DVFSC1}$	VDD1	11
	$IDD4W_{DVFSC2H}$	VDD2H	11
	$IDD4W_{DVFSC2L}$	VDD2L	8,11, 12
	$IDD4W_{DVFSCQ}$	VDDQ	4,11

All-bank REFRESH Burst current:
tCK = tCKmin;
CS is LOW between valid commands;
tRC = tRFCabmin;
Burst refresh;
CA bus inputs are switching;
Data bus inputs are stable;
RDQS_t is stable (if Link ECC is enabled)
ODT disabled
WCK inputs are stable and static
	$IDD5_1$	VDD1	

	$IDD5_{2H}$	VDD2H	
	$IDD5_{2L}$	VDD2L	8
	$IDD5_Q$	VDDQ	4

All-bank REFRESH Average current:
tCK = tCKmin;
CS is LOW between valid commands;
tRC = tREFI;
CA bus inputs are switching;
Data bus inputs are stable;
RDQS_t is stable (if Link ECC is enabled)
ODT disabled
WCK inputs are stable and static
	$IDD5AB_1$	VDD1	

	$IDD5AB_{2H}$	VDD2H	
	$IDD5AB_{2L}$	VDD2L	8
	$IDD5AB_Q$	VDDQ	4

Parameter / Condition	Symbol	Power Supply	Note
All-bank REFRESH Burst current with E-DVFSC: tCK = 1.25ns (800 MHz) CKR=2:1 CS is LOW between valid commands; tRC = tRFCabmin; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is don't care. ODT disabled WCK inputs are stable and static Enhanced DVFSC mode is enabled	$IDD5_{ED1}$	VDD1	
	$IDD5_{ED2H}$	VDD2H	
	$IDD5_{ED2L}$	VDD2L	8
	$IDD5_{EDQ}$	VDDQ	4
All-bank REFRESH Average current with E-DVFSC: tCK = 1.25ns (800 MHz) CKR=2:1 CS is LOW between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is don't care. ODT disabled WCK inputs are stable and static Enhanced DVFSC mode is enabled	$IDD5AB_{ED1}$	VDD1	
	$IDD5AB_{ED2H}$	VDD2H	
	$IDD5AB_{ED2L}$	VDD2L	8
	$IDD5AB_{EDQ}$	VDDQ	4

Per-bank REFRESH Average current:
tCK = tCKmin;
CS is LOW between valid commands;
tRC = tREFI/8;
CA bus inputs are switching;
Data bus inputs are stable;
RDQS_t is stable (if Link ECC is enabled)
ODT disabled
WCK inputs are stable and static
	$IDD5PB_{1}$	VDD1	

	$IDD5PB_{2H}$	VDD2H	
	$IDD5PB_{2L}$	VDD2L	8
	$IDD5PB_{Q}$	VDDQ	4
Per-bank REFRESH Average current with E-DVFSC: tCK = 1.25ns (800 MHz) CKR=2:1 CS is LOW between valid commands; tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; RDQS_t is don't care. ODT disabled WCK inputs are stable and static Enhanced DVFSC mode is enabled	$IDD5PB_{ED1}$	VDD1	
	$IDD5PB_{ED2H}$	VDD2H	
	$IDD5PB_{ED2L}$	VDD2L	8
	$IDD5PB_{EDQ}$	VDDQ	4

Parameter / Condition	Symbol	Power Supply	Note
Power down Self refresh current: CK_t=LOW, CK_c=HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; (≤85° C) Maximum TBDx Self-Refresh Rate; (>85° C) RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	$IDD6_1$	VDD1	6,7
	$IDD6_{2H}$	VDD2H	6,7
	$IDD6_{2L}$	VDD2L	6,7,8
	$IDD6_Q$	VDDQ	4,6,7,8
Deep sleep mode current: CK_t=LOW, CK_c=HIGH; CS is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; (≤85° C) Maximum TBDx Self-Refresh Rate; (>85° C) RDQS_t is stable (if Link ECC is enabled) ODT disabled WCK inputs are stable and static	$IDD6_{DS1}$	VDD1	6,7
	$IDD6_{DS2H}$	VDD2H	6,7
	$IDD6_{DS2L}$	VDD2L	6,7,8
	$IDD6_{DSQ}$	VDDQ	4,6,7

Note(s):

(1) Published IDD values are the maximum of the distribution of the arithmetic mean.

(2) ODT disabled. MR11 OP[6:4] = 000_B

(3) IDD current specifications are tested after the device is properly initialized.

(4) Measured currents are the summation of VDDQ and VDD2H / VDD2L.

(5) Guaranteed by design with output load = 5pF and RON = 40 ohm.

(6) The 1x Self-Refresh Rate is the rate at which the LPDDR5 device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.

(7) This is the general definition that applies to full array Self Refresh.

(8) When MR13 OP[7] is high, single VDD2 rail, VDD2L Current shall be added to VDD2H Current.

(9) IDD values can be different according to the bank organization set by MR3 OP[4:3].

(10) When DVFSC is enabled, the minimum tCK shall be set by following DVFSC operating frequency.

(11) IDD values can be different according to the DVFSC set by MR19 OP[1:0].

(12) When LPDDR5X SDRAM(MR8 OP[1:0]=01B) supports both DVFSC and E-DVFSC mode(MR41 OP[2:1]=10B), this IDD current at mode which consumes bigger VDD2L current than the other.

8.2 IDD Specification

IDD for 16Gb Single Die;VDD1=1.80V;VDD2H=1.05V;VDD2L=0.9V;VDDQ =0.5V.

Symbol		Supply	8533 Mb/s	Unit	Notes
			X16		
IDD0	IDD01	VDD1	3.80	mA	
	IDD02H	VDD2H	53.00	mA	
	IDD02L	VDD2L	0.20	mA	
	IDD0Q	VDDQ	0.60	mA	
IDD2P	IDD2P1	VDD1	1.50	mA	
	IDD2P2H	VDD2H	3.90	mA	
	IDD2P2L	VDD2L	0.20	mA	
	IDD2PQ	VDDQ	0.60	mA	
IDD2PS	IDD2PS1	VDD1	1.50	mA	
	IDD2PS2H	VDD2H	3.90	mA	
	IDD2PS2L	VDD2L	0.20	mA	
	IDD2PSQ	VDDQ	0.60	mA	
IDD2N	IDD2N1	VDD1	1.50	mA	
	IDD2N2H	VDD2H	32.50	mA	
	IDD2N2L	VDD2L	0.20	mA	
	IDD2NQ	VDDQ	0.60	mA	
IDD2NS	IDD2NS1	VDD1	1.50	mA	
	IDD2NS2H	VDD2H	32.50	mA	
	IDD2NS2L	VDD2L	0.20	mA	
	IDD2NSQ	VDDQ	0.60	mA	
IDD3P	IDD3P1	VDD1	2.50	mA	
	IDD3P2H	VDD2H	12.50	mA	
	IDD3P2L	VDD2L	0.20	mA	
	IDD3PQ	VDDQ	0.60	mA	
IDD3PS	IDD3PS1	VDD1	2.50	mA	
	IDD3PS2H	VDD2H	12.50	mA	
	IDD3PS2L	VDD2L	0.20	mA	
	IDD3PSQ	VDDQ	0.60	mA	
IDD3N	IDD3N1	VDD1	2.80	mA	
	IDD3N2H	VDD2H	40.00	mA	
	IDD3N2L	VDD2L	0.20	mA	
	IDD3NQ	VDDQ	0.60	mA	

Symbol		Supply	8533 Mb/s	Unit	Notes
			X16		
IDD3NS	IDD3NS1	VDD1	2.80	mA	
	IDD3NS2H	VDD2H	40.00	mA	
	IDD3NS2L	VDD2L	0.20	mA	
	IDD3NSQ	VDDQ	0.60	mA	
IDD4R	IDD4R1	VDD1	20.50	mA	3,4,6
	IDD4R2H	VDD2H	430.00	mA	3,4,6
	IDD4R2L	VDD2L	0.20	mA	3,4,6
	IDD4RQ	VDDQ	121.00	mA	3,4,6
IDD4W	IDD4W1	VDD1	18.50	mA	3,6
	IDD4W2H	VDD2H	280.00	mA	3,6
	IDD4W2L	VDD2L	0.20	mA	3,6
	IDD4WQ	VDDQ	0.60	mA	3,6
IDD5	IDD51	VDD1	24.00	mA	
	IDD52H	VDD2H	205.00	mA	
	IDD52L	VDD2L	0.20	mA	
	IDD5Q	VDDQ	0.60	mA	
IDD5AB	IDD5AB1	VDD1	3.60	mA	
	IDD5AB2H	VDD2H	47.00	mA	
	IDD5AB2L	VDD2L	0.20	mA	
	IDD5ABQ	VDDQ	0.60	mA	
IDD5PB	IDD5PB1	VDD1	3.60	mA	
	IDD5PB2H	VDD2H	47.00	mA	
	IDD5PB2L	VDD2L	0.20	mA	
	IDD5PBQ	VDDQ	0.60	mA	

Note(s):

(1) Published IDD values except IDD4RQ are the maximum IDD values considering the worst-case conditions of process, temperature, and voltage.

(2) BG mode. DVFSC and DVFSQ disabled.

(3) BL = 16, DBI disabled.

(4) IDD4RQ value is reference only. Typical value. Output load = 5pF; RON = 40 ohms; TC = 25°C.

(5) VDD1 = 1.70–1.95V; VDD2H = 1.01–1.12V; VDD2L = 0.87–0.97V; VDDQ = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled); TC = –25°C to +85°C

(6) IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.

(7) Notes 1, 2, and 5 apply to entire table.

Symbol		Supply	8533 Mb/s	Unit	Notes
			X16		
IDD4R-DVFSC	IDD4R-DVFSC1	VDD1	10.00	mA	3,4,6
	IDD4R-DVFSC2H	VDD2H	32.00	mA	3,4,6
	IDD4R-DVFSC2L	VDD2L	115.00	mA	3,4,6
	IDD4R-DVFSCQ	VDDQ	74.70	mA	3,4,6
IDD4W-DVFSC	IDD4W-DVFSC1	VDD1	9.00	mA	3,6
	IDD4W-DVFSC2H	VDD2H	29.00	mA	3,6
	IDD4W-DVFSC2L	VDD2L	80.00	mA	3,6
	IDD4W-DVFSCQ	VDDQ	0.60	mA	3,6
IDD5ED	IDD5ED1	VDD1	21.00	mA	
	IDD5ED2H	VDD2H	160.00	mA	
	IDD5ED2L	VDD2L	26.50	mA	
	IDD5EDQ	VDDQ	0.60	mA	
IDD5ABED	IDD5ABED1	VDD1	3.40	mA	
	IDD5ABED2H	VDD2H	24.00	mA	
	IDD5ABED2L	VDD2L	22.00	mA	
	IDD5ABEDQ	VDDQ	0.60	mA	
IDD5PBED	IDD5PBED1	VDD1	3.40	mA	
	IDD5PBED2H	VDD2H	24.00	mA	
	IDD5PBED2L	VDD2L	22.00	mA	
	IDD5PBEDQ	VDDQ	0.60	mA	

Note(s):

(1) Published IDD values except IDD4RQ are the maximum IDD values considering the worst-case conditions of process, temperature, and voltage.

(2) BG mode. DVFSC and DVFSQ disabled.

(3) BL = 16, DBI disabled.

(4) IDD4RQ value is reference only. Typical value. Output load = 5pF; RON = 40 ohms; TC = 25°C.

(5) VDD1 = 1.70–1.95V; VDD2H = 1.01–1.12V; VDD2L = 0.87–0.97V; VDDQ = 0.47–0.57V (DVFSQ disabled)/0.27-0.37V (DVFSQ enabled); TC = –25°C to +85°C

(6) IDD4R2 and IDD4W2 have implemented a more stringent pattern than required by JEDEC and therefore these IDD values are slightly higher than if the JEDEC pattern was used.

(7) Notes 1, 2, and 5 apply to entire table.

Symbol		Supply	8533 Mb/s	Unit	Notes
			X16		
IDD6 (25°C)	IDD61	VDD1	0.27	mA	
	IDD62H	VDD2H	1.00	mA	
	IDD62L	VDD2L	2.00	µA	
	IDD6Q	VDDQ	30.00	µA	
IDD6 (85°C)	IDD61	VDD1	3.70	mA	
	IDD62H	VDD2H	21.00	mA	
	IDD62L	VDD2L	0.20	mA	
	IDD6Q	VDDQ	0.60	mA	
IDD6DS (25°C)	IDD6DS1	VDD1	0.27	mA	
	IDD6DS2H	VDD2H	1.00	mA	
	IDD6DS2L	VDD2L	2.00	µA	
	IDD6DSQ	VDDQ	30.00	µA	
IDD6DS (85°C)	IDD6DS1	VDD1	3.70	mA	
	IDD6DS2H	VDD2H	21.00	mA	
	IDD6DS2L	VDD2L	0.20	mA	
	IDD6DSQ	VDDQ	0.60	mA	

Note(s):

(1) IDD6 25°C is the typical value in the distribution with nominal VDD and a reference-only value. IDD6 85°C is the maximum IDD guaranteed value considering the worst-case conditions of process, temperature, and voltage.

(2) DVFSC and DVFSQ disabled.

(3) VDD1 = 1.70–1.95V; VDD2H = 1.01–1.12V; VDD2L = 0.87–0.97V; VDDQ = 0.47–0.57V; TC = –25°C to +85°C

(4) While entering and exiting self-refresh modes, all defined/used supply rails (VDD1, VDD2H, VDD2L, VDDQ) are required to be at valid levels. After the self-refresh with power down mode entrance commands are completed and tESPD timing requirement has been satisfied, the VDDQ power rail may be turned off by the controller.

9.0 Electrical Characteristics and AC Timing

9.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR5 device.

9.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200-cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCKj\right) / N$$

$$\text{where N} = 200$$

Unit "tCK(avg)" represents the actual clock average tCK(avg) of the input clock under operation. Unit "nCK" represents one clock cycle of the input clock, counting the actual clock edges. tCK(avg) may change by up to +/-1% within a 100-clock cycle window, provided that all jitter and timing specs are met.

9.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.

9.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCHj\right) / (N \times tCK(avg))$$

$$\text{where N} = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = (\sum_{j=1}^{N} tCLj) / (N \times tCK(avg))$$

$$\text{where N} = 200$$

9.1.4 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

9.1.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.

tJIT(per),act is the actual clock jitter for a given system.

tJIT(per),allowed is the specified allowed clock period jitter.

tJIT(per) is not subject to production test.

9.1.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

tJIT(cc) = Max of |{tCK(i +1) - tCK(i)}|.

tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test.

9.1.7 Clock Timing

Clock AC Timings for 5/10/67/133MHz

Parameter	Symbol	5MHz		10MHz		67MHz		133MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Average clock period	tCK(avg)	200	200	100	200	14.93	200	7.5	200	ns
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)
Absolute clock period	tCK(abs)	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	ns
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)
Clock period jitter	tJIT(per)	-11200	11200	-5600	5600	-840	840	-430	430	ps
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	22400	-	11200	-	1680	-	860	ps

Clock AC Timings for 200/267/344/400MHz

Parameter	Symbol	200MHz		267MHz		344MHz		400MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Average clock period	tCK(avg)	5	200	3.75	200	2.9	200	2.5	200	ns
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)
Absolute clock period	tCK(abs)	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	ns
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)
Clock period jitter	tJIT(per)	-280	280	-210	210	-170	170	-140	140	ps
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	560	-	420	-	340	-	280	ps

Clock AC Timings for 467/533/600/688

Parameter	Symbol	467MHz		533MHz		600MHz		688MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Average clock period	tCK(avg)	2.15	200	1.875	200	1.667	200	1.453	200	ns
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)
Absolute clock period	tCK(abs)	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	ns
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)
Clock period jitter	tJIT(per)	-120	120	-110	110	-95	95	-85	85	ps
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	240	-	220	-	190	-	170	ps

Clock AC Timings for 750/800/937.5/1066MHz

Parameter	Symbol	750MHz		800MHz		937.5MHz		1066.5MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Average clock period	tCK(avg)	1.333	200	1.25	200	1066.7	200ns	937.6	200ns	ns
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK (avg)
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK (avg)
Absolute clock period	tCK(abs)	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	tCK (avg) MIN + tJIT (per) MIN	-	ns
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK (avg)
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tCK (avg)
Clock period jitter	tJIT(per)	-75	75	-70	70	-60	60	-55	55	ps
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	150	-	140	-	120	-	110	ps

9.2 Write Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input write clocks violating the min/max values may result in malfunction of the LPDDR5 device.

9.2.1 Definition for tWCK(avg) and nWCK

tWCK(avg) is calculated as the average write clock period across any consecutive 200 cycle window, where each write clock period is calculated from rising edge to rising edge.

$$tWCK(avg) = \left(\sum_{j=1}^{N} tWCKj\right) / N$$

$$\text{where N} = 200$$

Unit "tWCK(avg)" represents the actual write clock average tWCK(avg) of the input write clock under operation. Unit "nWCK" represents one write clock cycle of the input write clock, counting the actual write clock edges. tWCK(avg) may change by up to +/-1% within a 100 write clock cycle window, provided that all jitter and timing specs are met.

9.2.2 Definition for tWCK(abs)

tWCK(abs) is defined as the absolute write clock period, as measured from one rising edge to the next consecutive rising edge.
tWCK(abs) is not subject to production test.

9.2.3 Definition for tWCH(avg) and tWCL(avg)

tWCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tWCH(avg) = \left(\sum_{j=1}^{N} tWCHj\right) / (N \times tWCK(avg))$$

$$\text{where N} = 200$$

tWCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tWCL(avg) = \left(\sum_{j=1}^{N} tWCLj\right) / (N \times tWCK(avg))$$

$$\text{where N} = 200$$

9.2.4 Definition for tWCH(abs) and tWCL(abs)

tWCH(abs) is the absolute instantaneous write clock high pulse width, as measured from one rising edge to the following falling edge. tWCL(abs) is the absolute instantaneous write clock low pulse width, as measured from one falling edge to the following rising edge. Both tWCH(abs) and tWCL(abs) are not subject to production test.

9.2.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tWCK from tWCK(avg).

tJIT(per) = Min/max of {tWCKi - tWCK(avg) where i = 1 to 200}.

tJIT(per), act is the actual write clock jitter for a given system.

tJIT(per), allowed is the specified allowed write clock period jitter.

tJIT(per) is not subject to production test.

9.2.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in write clock period between two consecutive write clock cycles.

tJIT(cc) = Max of |{tWCK(i +1) - tWCK(i)}|.

tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test

9.2.7 Definition for tERR(2per)

tERR(2per) is defined as the cumulative error across 2 consecutive cycles from tWCK(avg).

tERR(2per) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tWCKj\right) - n \times tWCK(avg)$$

$$\text{where N} = 2$$

9.2.8 Definition for tERR(3per)

tERR(3per) is defined as the cumulative error across 3 consecutive cycles from tWCK(avg).
tERR(3per) is not subject to production test

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tWCKj \right) - n \times tWCK(avg)$$

where N = 3

9.2.9 Definition for tERR(4per)

tERR(4per) is defined as the cumulative error across 4 consecutive cycles from tWCK(avg).
tERR(4per) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tWCKj \right) - n \times tWCK(avg)$$

where N = 4

9.2.10 Write Clock Timing

Write Clock AC Timings for 266/533/800/1067MHz

Parameter	Symbol	266MHz		533MHz		800MHz		1067MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Clock Timing										
Average Write Clock period	tWCK (avg)	3.76	50	1.877	50	1.25	50	0.938	50	ns
Average High pulse width	tWCKH (avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tWCK (avg)
Average Low pulse width	tWCKL (avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tWCK (avg)
Absolute Write Clock period	tWCK (abs)	tWCK (avg) MIN + tJIT (per) MIN	-	tWCK (avg) MIN + tJIT (per) MIN	-	tWCK (avg) MIN + tJIT (per) MIN	-	tWCK (avg) MIN + tJIT (per) MIN	-	ns
Absolute High Write Clock pulse width	tWCKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)
Absolute Low Write Clock pulse width	tWCKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-190	190	-95	95	-70	70	-56	56	ps
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	380	-	190	-	140	-	112	ps
Cumulative error across 2 cycles	tERR (2per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 3 cycles	tERR (3per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

Parameter	Symbol	266MHz		533MHz		800MHz		1067MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Clock Timing										
Cumulative error across 4 cycles	tERR (4per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

Write Clock AC Timings for 1375/1600/1867/2134MHz

Parameter	Symbol	1375MHz		1600MHz		1867MHz		2134MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Clock Timing										
Average Write Clock period	tWCK (avg)	0.728	50	0.625	50	0.536	50	0.469	50	ns
Average High pulse width	tWCKH (avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tWCK (avg)
Average Low pulse width	tWCKL (avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tWCK (avg)
Absolute Write Clock period	tWCK (abs)	tWCK (avg) MIN + tJIT (per) MIN	-	tWCK (avg) MIN + tJIT (per) MIN	-	tWCK (avg) MIN + tJIT (per) MIN	-	tWCK (avg) MIN + tJIT (per) MIN	-	ns
Absolute High Write Clock pulse width	tWCKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)
Absolute Low Write Clock pulse width	tWCKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-46	46	-40	40	-34	34	-30	30	ps

Parameter	Symbol	1375MHz		1600MHz		1867MHz		2134MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Clock Timing										
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	92	-	80	-	68	-	60	ps
Cumulative error across 2 cycles	tERR (2per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 3 cycles	tERR (3per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 4 cycles	tERR (4per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

Write Clock AC Timings for 2400/2750/3000/3200MHz

Parameter	Symbol	2400MHz		2750MHz		3000MHz		3200MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Clock Timing										
Average Write Clock period	tWCK (avg)	0.417	50	0.364	50	0.334	50	0.313	50	ns
Average High pulse width	tWCKH (avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tWCK (avg)
Average Low pulse width	tWCKL (avg)	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tWCK (avg)
Absolute Write Clock period	tWCK (abs)	tWCK (avg) MIN + tJIT (per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT (per) MIN	-	tWCK (avg) MIN + tJIT (per) MIN	-	ns
Absolute High Write Clock pulse width	tWCKH (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)

Parameter	Symbol	2400MHz		2750MHz		3000MHz		3200MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Clock Timing										
Absolute Low Write Clock pulse width	tWCKL (abs)	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	tWCK (avg)
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-28	28	-26	26	-24	24	-22	22	ps
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	56	-	52	-	48	-	44	ps
Cumulative error across 2 cycles	tERR (2per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 3 cycles	tERR (3per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 4 cycles	tERR (4per)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

Write Clock AC Timings for 3750/4266.5MHz

Parameter	Symbol	3750MHz		4266.5MHz		Units
		Min	Max	Min	Max	
Write Clock Timing						
Average Write Clock period	tWCK(avg)	266.7ps	50ns	234.4ps	50ns	-
Average High pulse width	tWCKH(avg)	0.46	0.54	0.46	0.54	tWCK(avg)
Average Low pulse width	tWCKL(avg)	0.46	0.54	0.46	0.54	tWCK(avg)

Parameter	Symbol	3750MHz		4266.5MHz		Units
		Min	Max	Min	Max	
Write Clock Timing						
Absolute Write Clock period	tWCK(abs)	tWCK (avg) MIN + tJIT(per) MIN	-	tWCK (avg) MIN + tJIT(per) MIN	-	ns
Absolute High Write Clock pulse width	tWCKH(abs)	0.43	0.57	0.43	0.57	tWCK (avg)
Absolute Low Write Clock pulse width	tWCKL(abs)	0.43	0.57	0.43	0.57	tWCK (avg)
Write Clock period jitter tJIT(per)	WCK period jitter tJIT(per)	-19	19	-17	17	ps
Maximum Write Clock Jitter between consecutive cycles	tJIT(cc)	-	38	-	34	ps
Cumulative error across 2 cycles	tERR(2per)	TBD	TBD	TBD	TBD	ps
Cumulative error across 3 cycles	tERR(3per)	TBD	TBD	TBD	TBD	ps
Cumulative error across 4 cycles	tERR(4per)	TBD	TBD	TBD	TBD	ps

10.0 DRAM IC Marking P/N Decoder

L5	EG	32	D4	023	M	C	A	S
1-2	3-4	5-6	7-8	9-11	12	13	14	15

1-2: DRAM IC Type

L5= LPDDR5/5X

3-4: Capacity

AG= 16Gb

CG= 32Gb

EG= 64Gb

5-6: IC Configuration

32= x32

64= x64

7-8: DIE Count

D2= 2 die (DDP)

D4= 4 die (QDP)

D8= 8 die (ODP)

9-11: Speed

031= 6400 (313ps)

026= 7500 (267ps)

023= 8533 (234ps)

12: DIE Vendor

M= Micron

13: DIE Version

A= A DIE

B= B DIE

C= C DIE

14: PKG Type

A= 315 Ball FBGA

15: OP. Temp

S= -25°C ~ 85°C

I= -40°C ~ 95°C