MEGAHUNT

MH1903
Brief Introduction

Highly Integrated Secure SOC

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Megahunt Tehnologies Inc.

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Date	Revision	Description	Author
2018-12-3	1.00	First draft completed	MEGAHUNT
2018-12-14	1.10	Delete PD6, PD7 ALT0 multiplexing function	MEGAHUNT
2019-03-01	1.20	Delete QFP176 package information	MEGAHUNT
2019-04-18	1.30	Modify PD8 Multiplexing	MEGAHUNT
2019-05-05	1.40	Adding BGA121 Packaging Information	MEGAHUNT

1 Chip Overview

1.1 Chip Description

The MH1903 chip uses the 32bit processor. Leveraging its superior architectural features, high performance and low cost, it provides a high-performance, secure, energy-efficient solution.

Chip built-in hardware security encryption module to support a variety of encryption and security algorithms, including DES, TDES, AES, RSA, SHA mainstream encryption algorithm. Chip hardware also supports a variety of attack detection, in line with financial security equipment standards.

The chip contains a secure BOOT program to support download, RSA signature verification when starting the firmware. The chip has built-in 1MB SRAM, and also integrates a wealth of peripheral resources: Smartcard, magnetic stripe card decoding, security keyboard, LCDI, all peripheral driver software compatible with the current mainstream security chip software interface, the user can do a rapid development and transplantation on the basis of existing programs.

1.2 Main Features

- Processor
  - 32-bit RISC Core
  - MPU memory protection unit
  - Maximum 204MHz main frequency (1, 2 frequency adjustable)
  - FPU unit
  - 1 controlled JTAG-DP/SW-DP debug port
- 1MB SRAM
- 1 QSPI controller
- 1 PSRAM controller
- 1 SDRAM controller
- System control module (controls all peripheral modules and system-related clock configuration)
- Secure Encryption Algorithm Acceleration Engine

- Symmetric algorithm: DES, TDES, AES-128/192/256
- Asymmetric algorithm: RSA-1024/2048、ECC
- HASH check algorithm: SHA-1/224/256/384/512

- 3 SmartCard interfaces (support EMV Level-1 protocol specification, ISO7816-3 standard)
- 4 UART interfaces (both support 4 lines)
- 5 SPI interfaces (1 master-slave can be configured, 4 master interfaces)
- One IIC interface
- One KBD (4x5 matrix keyboard)
- 8 32-bit TIMER (with PWM function, support for single-cycle output)
- One LCDI interface, support 8080, 6800 bus protocol
- One true random number generator
- One DMA controller (supports 8-channel DMA transfer)
- One CRC module (supports 16Bit/32Bit, a variety of commonly used polynomial calculation)
- Support up to 128 GPIOs
- Supports up to 8 static Tamper or 4 dynamic Tamper (4 outputs, 4 inputs), dynamic/static compatible
- A group of internal sensor (supports high and low voltage, high and low temperature, Mesh, clock and voltage glitch detection)
- One block of key storage area (supports hardware quick wipe)
- One USB (OTG-FS)
  - Support USB2.0 and OTG1.0a
  - Built-in USB PHY module
  - Dedicated DMA channels and proprietary interrupt vectors to speed up data communication
- Integrated internal watchdog
- 1 10bit DAC interface
- One 6-channel 12-bit ADC, supports up to 857KHz sampling rate (0 channel 0 ~ 5 V, 1- 5 channel 0 ~ 1.8 V)
- Support for magnetic stripe decoding, support for standard cards such as ISO/ABA, AAMVA, IBM and JIS II

- One DCMI interface
- One SDIO Host interface
- One MIPI-CSI2 interface

1.3 Chip Application

Two-dimensional code scanning code terminals, simple POS machines and other financial security devices that have two-dimensional code scanning codes and are sensitive to power consumption and cost.

1.4 Chip Basic Structure Description

MH1903 chip includes security core, 1MB SRAM, system control module, security encryption module, one TRNG module, a 8-channel DMA controller, a USB interface, a GPIO module, one WDT module, one BPU module, 8 32bit Timers, one CRC module, 5 SPI interfaces, 3 SCI interfaces, 4 UART interfaces, one DAC, one 6-channel ADC, one SDRAM controller, one QSPI PRAM controller, one DCMI interface, one SDIO Host interface, one MIPI-CSI2 interface, The system block diagram is as follows:

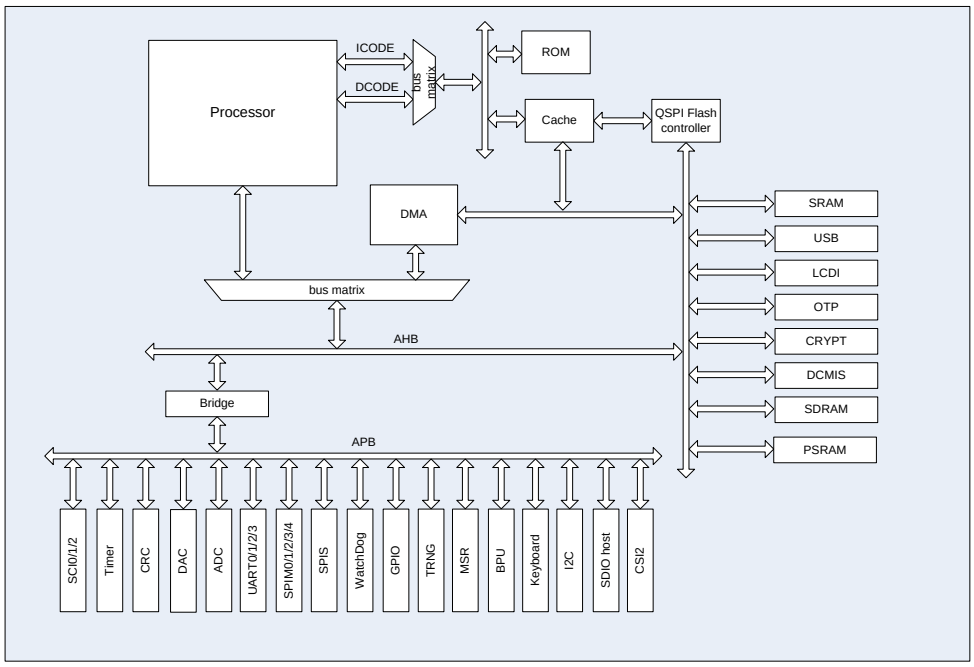

Figure 1 System Main Module

2 Chip Characteristics Description

2.1 Electrical Characteristics

Table 1 Limit Parameters

Parameter	Description	Range	Unit
VDD	Steady State Supply Voltage	-0.3 to 3.6	V
Iddpd	Shutdown current	--	nA
Tamb	Operating temperature	-40~+85	℃
Tstg	stored temperature	-40~+125	℃
Ground	Ground	-0.3~0.3	V
Voh	Digital output high level	VDD -0.3 ~ VDD+0.3	V
Vol	Digital output low level	<0.4	V
Ioh	Pull current	29.2	mA
Iol	Sink current	17	mA
Vih	Digital input high level	≥0.7×VDD	V
ViL	Digital input low level	≤0.3×VDD	V

Table 2 Electrical Characteristics

parameter	Conditions (-40°C to +85°C)	value		unit
		Min	Max	
AVD33		2.7	3.6	V
VDD33		2.7	3.6	V
VBAT33		2	3.6	V
Vol	VDD=3.3V	-	0.4	V
Voh	VDD=3.3V	VDD – 0.3	-	V
VIH	VDD=3.3V	0.7×VDD	-	V
VIL	VDD=3.3V	-	0.3×VDD	V

Table 3 Safety-related Features

sensor	Description	range	unit
Temperature Sensor	High temperature detection range	100±10	℃
	Low temperature detection range	-30~-40	℃
Voltage sensor	Main power supply voltage high voltage detection range	4.0±0.2	V

	Main power supply voltage low voltage detection range		2.8±0.1	V
	Battery voltage high voltage detection range		4.0±0.1	V
	Battery voltage low voltage detection range		1.9±0.1	V
Clock frequency sensor	12M clock frequency detection range		12±50%	MHz
	32K clock frequency detection range	High frequency	50.768±2	KHz
		Low frequency	20.768±2	KHz
External Tamper resistor	Pull-up Resistance on Tamper Pin		3.6M±10%	Ω

Table 4 Power Consumption List

Operating mode	Description	Power consumption	unit
RUN	● All peripherals are open		mA
	▪ core 204MHz, HCLK 102MHz, PCLK 51MHz	80	
	▪ core 192MHz, HCLK 96MHz, PCLK 48MHz	75	
	▪ core 168MHz, HCLK 84MHz, PCLK 42MHz	67	
	● All peripherals are closed		
	▪ core 204MHz, HCLK 102MHz, PCLK 51MHz	48	
	▪ core 192MHz, HCLK 96MHz, PCLK 48MHz	46	
	▪ core 168MHz, HCLK 84MHz, PCLK 42MHz	40	
CPU Sleep	All peripherals are closed 204@MHz	16.5	mA
Deep Sleep	●Support for IO low level wake-up	380	uA
VBAT	●Internal sensors are fully turned on		uA
	Main power failure	2.3	
	Main power supply	0.8	

2.2 Pin Definition

Table 5 MH1903 BGA169 9mm × 9mm Package Pin Definition

PIN No.	PIN Name	ATL0	ALT1 (default)	ATL2	ATL3	Remarks
A1	VBAT33					Battery power supply
A2	PA8	SCI0_CLK	PA[8]		SPI1_MOSI	
A3	XO32					XTAL 32K Output
A4	PA4		PA[4]	PWM4	XTAL32K	
A5	VDD12					
A6	PG11		PG[11]		MP_DATA14	
A7	XO12M					XTAL 12M Output
A8	PG10	PRAM_D3	PG[10]		MP_DATA13	
A9	ID					USB ID

A10	DN					USB DN
A11	VBUS					USB VBUS
A12	**MSR_IN1**					Magnetic stripe card T1+
A13	**MSR_IN2**					Magnetic stripe cardT1-
B1	PA7	SCI0_VCCEN	PA[7]	PWM7	SPI1_CSN0	
B2	PA9	SCI0_RSTN	PA[9]		SPI1_MISO	
B3	XI32					XTAL 32K Input
B4	PA5		PA[5]	PWM5	CLK_24M	Configurable output 24M
B5	**VDD33**					
B6	PG12		PG[12]		MP_DATA15	
B7	XI12M					XTAL 12M Input
B8	PG5	PRAM_CLK	PG[5]		MP_DATA8	
B9	PG7	PRAM_DATA0	PG[7]		MP_DATA10	
B10	DP					USB DP
B11	PG3	PWM6	PG[3]	CLK_24M	MP_DATA6	
B12	**MSR_IN3**					Magnetic stripe card T2+
B13	**MSR_IN4**					Magnetic stripe card T2-
C1	PA6	SCI0_DET	PA[6]	PWM6	SPI1_SCK	
C2	PE6	UART3_CTS	PE[6]	I2C0_SCL	MP_ADDR3	
C3	PE5	UART3_TX/IrDA_OUT	PE[5]		MP_ADDR2	
C4	**VSS**					
C5	PE4	UART3_RX/IrDA_IN	PE[4]		MP_ADDR1	
C6	PG9	PRAM_DATA2	PG[9]		MP_DATA12	
C7	PG8	PRAM_DATA1	PG[8]		MP_DATA11	
C8	PG6	PRAM_CSN	PG[6]		MP_DATA9	
C9	**VSS**					
C10	PG4	PWM7	PG[4]	CLK_24M	MP_DATA7	
C11	PG2	PWM5	PG[2]		MP_DATA5	
C12	**MSR_IN5**					Magnetic stripe card T3+
C13	**MSR_IN6**					Magnetic stripe card T3-
D1	PE7	UART3_RTS	PE[7]	I2C0_SDA	MP_ADDR4	
D2	QSPI_DATA0					
D3	PA10	SCI0_IO	PA[10]			
D4	PE3	SPI4_MISO	PE[3]		MP_ADDR0	
D5	**EXT4**					External Tamper4
D6	**EXT3**					External Tamper3
D7	PF10	KeyBoard6	PF[10]		MP_CS	

D8	PF11	KeyBoard7	PF[11]		MP_RAS	
D9	PF12	KeyBoard8	PF[12]	CLK_24M	MP_WE	
D10	PB6	DRV_VBUS	PB[6]	PWM6		
D11	QSPI_DATA2					
D12	**VDD33**					
D13	**VDD25**					1uF ground capacitance
E1	PE8	SCI2_DET	PE[8]	UART3_RX/IrDA_IN	MP_ADDR5	
E2	QSPI_CLK					
E3	PE12	SCI2_IO	PE[12]	SPI4_CLK	MP_ADDR9	
E4	**EXT0**					External Tamper0
E5	**EXT6**					External Tamper6
E6	**EXT5**					External Tamper5
E7	PF7	KeyBoard3	PF[7]	SPI2_MISO	MP_DQM2	
E8	PF8	KeyBoard4	PF[8]	XTAL32K	MP_DQM3	
E9	PF9	KeyBoard5	PF[9]		MP_CAS	
E10	PH13	DCMIS_PIX_CLK	PH[13]		MP_RP	
E11	**VSS**					
E12	PF15	PWM2	PF[15]		MP_DATA2	
E13	PF14	PWM1	PF[14]		MP_DATA1	
F1	PE11	SCI2_RSTN	PE[11]	UART3_RTS	MP_ADDR8	
F2	QSPI_DATA3					
F3	PE10	SCI2_CLK	PE[10]	UART3_CTS	MP_ADDR7	
F4	**EXT2**					External Tamper2
F5	**EXT1**					External Tamper1
F6	**EXT7**					External Tamper7
F7	PF4	KeyBoard0	PF[4]	SPI2_CLK	MP_CLK	
F8	PF5	KeyBoard1	PF[5]	SPI2_CSN	MP_DQM0	
F9	PF6	KeyBoard2	PF[6]	SPI2_MOSI	MP_DQM1	
F10	PH12	DCMIS_HSYNC	PH[12]		MP_DATA31	
F11	QSPI_DATA1					
F12	PC0	TRST	PC[0]	ADC_IN0	UART1_RX/IrDA_IN	
F13	PF13	PWM0	PF[13]		MP_DATA0	
G1	PE13		PE[13]	SPI4_CSN	MP_ADDR10	
G2	PE9	SCI2_VCCEN	PE[9]	UART3_TX/IrDA_OUT	MP_ADDR6	

G3	**VSS**					
G4	PE0	SPI4_CLK	PE[0]	KeyBoard4		
G5	PE2	SPI4_MOSI	PE[2]	KeyBoard6		
G6	PC7	LCD_DATA2	PC[7]	SCI0_VCCEN		
G7	PD13	UART2_TX/IrDA_OUT	PD[13]	KeyBoard1		
G8	PD12	UART2_RX/IrDA_IN	PD[12]	KeyBoard0		
G9	PC5	LCD_DATA0	PC[5]	ADC_IN5		
G10	PH11	DCMIS_VSYNC	PH[11]		MP_DATA30	
G11	QSPI_CSN					
G12	PC1	TDI	PC[1]	ADC_IN1/DAC	UART1_TX/IrDA_OUT	
G13	MIPI_CLKN					
H1	PF1	SPI3_CSN	PF[1]	PWM5	MP_ADDR14	
H2	VDD33					
H3	PF0	SPI3_CLK	PF[0]	PWM4	MP_ADDR13	
H4	PE1	SPI4_CSN	PE[1]	KeyBoard5		
H5	PE14		PE[14]	SPI4_MOSI	MP_ADDR11	
H6	PC8	LCD_DATA3	PC[8]	SCI0_CLK		
H7	PD14	UART2_CTS	PD[14]	KeyBoard2		
H8	PC15	LCD_CD	PC[15]	SPI0_MISO		
H9	PD10	SPI3_MOSI	PD[10]	KeyBoard7		
H10	PG1	PWM4	PG[1]		MP_DATA4	
H11	PH10	DCMIS_DATA13	PH[10]		MP_DATA29	
H12	PC2	TDO	PC[2]	ADC_IN2	UART1_CTS	
H13	MIPI_CLKP					
J1	PF2	SPI3_MOSI	PF[2]	PWM6	MP_ADDR15	
J2	PF3	SPI3_MISO	PF[3]	PWM7	MP_CKE	
J3	PA1	UART0_TX/IrDA_OUT	PA[1]	PWM1		
J4	PE15		PE[15]	SPI4_MISO	MP_ADDR12	
J5	PA11	SCI1_DET	PA[11]		CLK_24M	
J6	PC6	LCD_DATA1	PC[6]	SCI0_DET		
J7	PD15	UART2_RTS	PD[15]	KeyBoard3		
J8	PC14	LCD_WR	PC[14]	SPI0_MOSI		
J9	PD11	SPI3_MISO	PD[11]	KeyBoard8		

J10	PG0	PWM3	PG[0]		MP_DATA3	
J11	PH9	DCMIS_DATA12	PH[9]		MP_DATA28	
J12	PC3	TMS	PC[3]	ADC_IN3	UART1_RTS	
J13	**MIPI_DATA0P**					
K1	PD1		PD[1]	SDIO_D1		
K2	PD0	DRV_VBUS	PD[0]	SDIO_D0		
K3	PA3	UART0_RTS	PA[3]	PWM3	I2C0_SDA	
K4	PA0	UART0_RX/IrDA_IN	PA[0]	PWM0		
K5	PB2	SPI2_SCK	PB[2]	PWM2	UART2_RX/IrDA_IN	
K6	PC9	**LCD_DATA4**	PC[9]	SCI0_RSTN		
K7	PC10	**LCD_DATA5**	PC[10]	SCI0_IO		
K8	PC13	**LCD_RD**	PC[13]	SPI0_CSN0		
K9	PC12	**LCD_DATA7**	PC[12]	SPI0_SCK		
K10	PC11	**LCD_DATA6**	PC[11]	XTAL32K		
K11	**VSS**					
K12	PC4	TCK	PC[4]	ADC_IN4	XTAL32K	
K13	**MIPI_DATA0N**					
L1	PD3		PD[3]	SDIO_D3		
L2	PD2		PD[2]	SDIO_D2		
L3	**VSS**					
L4	PA2	UART0_CTS	PA[2]	PWM2	I2C0_SCL	
L5	PB3	SPI2_CSN	PB[3]	PWM3	UART2_TX/IrDA_OUT	
L6	PG13	DCMIS_DATA0	PG[13]		MP_DATA16	
L7	PH2	DCMIS_DATA5	PH[2]		MP_DATA21	
L8	**VSS**					
L9	PH7	DCMIS_DATA10	PH[7]		MP_DATA26	
L10	PB12	SPI0_CLK	PB[12]	PWM3	UART1_RX/IrDA_IN	Independent power pin
L11	PH8	DCMIS_DATA11	PH[8]		MP_DATA27	
L12	**VDD33**					
L13	**MIPI_REXT**					Connect 6.04K to ground resistance

M1	PB0	I2C0_SCL	PB[0]	PWM0	XTAL32K	
M2	**VDD33**					
M3	PD5	UART1_TX/IrDA_OUT	PD[5]	SDIO_CCLK		
M4	**VDD33**					
M5	PB4	SPI2_MOSI	PB[4]	PWM4	UART2_CTS	
M6	PG14	DCMIS_DATA1	PG[14]		MP_DATA17	
M7	PH1	DCMIS_DATA4	PH[1]		MP_DATA20	
M8	PH4	DCMIS_DATA7	PH[4]		MP_DATA23	
M9	PH6	DCMIS_DATA9	PH[6]		MP_DATA25	
M10	IO_VCC					PB12~PB15 Pin power input
M11	PB13	SPI0_CSN	PB[13]	PWM4	UART1_TX/IrDA_OUT	Independent power pin
M12	PD8	SPI3_CLK	PD[8]	UART2_RX/IrDA_IN		
M13	REFP					1uF ground capacitance
N1	PB1	I2C0_SDA	PB[1]	PWM1	CLK_24M	
N2	PD4	UART1_RX/IrDA_IN	PD[4]	SDIO_CCMD		
N3	PD6		PD[6]	SDIO_SINT_N		
N4	PD7		PD[7]	SDIO_CDET_N		
N5	PB5	SPI2_MISO	PB[5]	PWM5	UART2_RTS	
N6	PG15	DCMIS_DATA2	PG[15]		MP_DATA18	
N7	PH0	DCMIS_DATA3	PH[0]		MP_DATA19	
N8	PH3	DCMIS_DATA6	PH[3]		MP_DATA22	
N9	PH5	DCMIS_DATA8	PH[5]		MP_DATA24	
N10	PB14	SPI0_MOSI	PB[14]	PWM5	UART1_CTS	Independent power pin
N11	PB15	SPI0_MISO	PB[15]	PWM6	UART1_RTS	
N12	PD9	SPI3_CSN	PD[9]	UART2_TX/IrDA_OUT		
N13	RSTN					Reset pin

Table 6 MH1903 BGA121 8mm × 8mm Package Pin Definition

PIN Name	PIN No.	ALT0	ALT1	ALT2	ALT3	Remarks
QSPI_DATA0	C1					
QSPI_DATA1	C11					
QSPI_DATA2	B11					
QSPI_DATA3	E1					
QSPI_CLK	D1					
QSPI_CSN	D11					
DCMIS_PIX_CLK	L7	DCMIS_PIX_CLK	PH[13]			
DCMIS_HSYNC	L6	DCMIS_HSYNC	PH[12]			
DCMIS_VSYNC	K6	DCMIS_VSYNC	PH[11]			
DCMIS_DATA0	K2	DCMIS_DATA0	PG[13]			
DCMIS_DATA1	H3	DCMIS_DATA1	PG[14]			
DCMIS_DATA2	J3	DCMIS_DATA2	PG[15]			
DCMIS_DATA3	L3	DCMIS_DATA3	PH[0]			
DCMIS_DATA4	H4	DCMIS_DATA4	PH[1]			
DCMIS_DATA5	J4	DCMIS_DATA5	PH[2]			
DCMIS_DATA6	K4	DCMIS_DATA6	PH[3]			
DCMIS_DATA7	L4	DCMIS_DATA7	PH[4]			
DCMIS_DATA8	H5	DCMIS_DATA8	PH[5]			
DCMIS_DATA9	J5	DCMIS_DATA9	PH[6]			
DCMIS_DATA10	K5	DCMIS_DATA10	PH[7]			
DCMIS_DATA11	L5	DCMIS_DATA11	PH[8]			
DCMIS_DATA12	H6	DCMIS_DATA12	PH[9]			
DCMIS_DATA13	J6	DCMIS_DATA13	PH[10]			
LCD_DATA0	B7	LCD_DATA0	PC[5]	ADC_IN5		
LCD_DATA1	K7	LCD_DATA1	PC[6]	SCI0_DET		
LCD_DATA2	H7	LCD_DATA2	PC[7]	SCI0_VCCEN		
LCD_DATA3	J7	LCD_DATA3	PC[8]	SCI0_CLK		
LCD_DATA4	G7	LCD_DATA4	PC[9]	SCI0_RSTN		
LCD_DATA5	G8	LCD_DATA5	PC[10]	SCI0_IO		
LCD_DATA6	J11	LCD_DATA6	PC[11]	XTAL32K		
LCD_DATA7	K10	LCD_DATA7	PC[12]	SPI0_SCK		
LCD_RD	K11	LCD_RD	PC[13]	SPI0_CSN0		
LCD_WR	L10	LCD_WR	PC[14]	SPI0_MOSI		
LCD_CD	L11	LCD_CD	PC[15]	SPI0_MISO		
KeyBoard0	D5	KeyBoard0	PF[4]	SPI2_CLK		
KeyBoard1	D6	KeyBoard1	PF[5]	SPI2_CSN		
KeyBoard2	D7	KeyBoard2	PF[6]	SPI2_MOSI		

KeyBoard3	D8	KeyBoard3	PF[7]	SPI2_MISO		
KeyBoard4	C9	KeyBoard4	PF[8]	XTAL32K		
KeyBoard5	D9	KeyBoard5	PF[9]			
KeyBoard6	E9	KeyBoard6	PF[10]			
KeyBoard7	E8	KeyBoard7	PF[11]			
KeyBoard8	F8	KeyBoard8	PF[12]	CLK_24M		
SCI0_CLK	B2	SCI0_CLK	PA[8]		SPI1_MOSI	
SCI0_VCCEN	A3	SCI0_VCCEN	PA[7]	PWM7	SPI1_CSN0	
SCI0_RSTN	C2	SCI0_RSTN	PA[9]		SPI1_MISO	
SCI0_DET	E2	SCI0_DET	PA[6]	PWM6	SPI1_SCK	
SCI0_IO	C3	SCI0_IO	PA[10]			
SCI2_DET	D3	SCI2_DET	PE[8]	UART3_RX/IrDA_IN		
SCI2_IO	G3	SCI2_IO	PE[12]	SPI4_CLK		
SCI2_RSTN	G2	SCI2_RSTN	PE[11]	UART3_RTS		
SCI2_CLK	G1	SCI2_CLK	PE[10]	UART3_CTS		
SCI2_VCCEN	E3	SCI2_VCCEN	PE[9]	UART3_TX/IrDA_OUT		
UART0_RX/IrDA_IN	D4	UART0_RX/IrDA_IN	PA[0]	PWM0		
UART0_TX/IrDA_OUT	E4	UART0_TX/IrDA_OUT	PA[1]	PWM1		
UART0_CTS	F4	UART0_CTS	PA[2]	PWM2	I2C0_SCL	
UART0_RTS	G4	UART0_RTS	PA[3]	PWM3	I2C0_SDA	
SPI2_SCK	K1	SPI2_SCK	PB[2]	PWM2	UART2_RX/IrDA_IN	
SPI2_MOSI	H2	SPI2_MOSI	PB[4]	PWM4	UART2_CTS	
SPI2_MISO	J2	SPI2_MISO	PB[5]	PWM5	UART2_RTS	
SPI2_CSN	L1	SPI2_CSN	PB[3]	PWM3	UART2_TX/IrDA_OUT	
SPI0_CLK	H8	SPI0_CLK	PB[12]	PWM3	UART1_RX/IrDA_IN	Independent power pin
SPI0_MOSI	K8	SPI0_MOSI	PB[14]	PWM5	UART1_CTS	
SPI0_MISO	L8	SPI0_MISO	PB[15]	PWM6	UART1_RTS	
SPI0_CSN	J8	SPI0_CSN	PB[13]	PWM4	UART1_TX/IrDA_OUT	
SPI3_CLK	E11	SPI3_CLK	PD[8]	UART2_RX/IrDA_IN		
SPI3_MOSI	G11	SPI3_MOSI	PD[10]	KeyBoard7		
SPI3_MISO	H11	SPI3_MISO	PD[11]	KeyBoard8		

SPI3_CSN	F11	SPI3_CSN	PD[9]	UART2_TX/IrDA_OUT		
PWM6	C7	PWM6	PG[3]	CLK_24M		Configurable output 24M
PWM7	C4	PWM7	PG[4]	CLK_24M		Configurable output 24M
ADC_IN0	B10	TRST	PC[0]	ADC_IN0	UART1_RX/IrDA_IN	
ADC_IN1/DAC	A9	TDI	PC[1]	ADC_IN1/DAC	UART1_TX/IrDA_OUT	
ADC_IN2	C10	TDO	PC[2]	ADC_IN2	UART1_CTS	
ADC_IN3	C8	TMS	PC[3]	ADC_IN3	UART1_RTS	
ADC_IN4	D10	TCK	PC[4]	ADC_IN4	XTAL32K	
I2C0_SCL	H1	I2C0_SCL	PB[0]	PWM0	XTAL32K	
I2C0_SDA	J1	I2C0_SDA	PB[1]	PWM1	CLK_24M	
MSR_IN1	H10					Magnetic stripe card T1+
MSR_IN2	G10					Magnetic stripe card T1-
MSR_IN3	H9					Magnetic stripe card T2+
MSR_IN4	G9					Magnetic stripe card T2-
MSR_IN5	F10					Magnetic stripe card T3+
MSR_IN6	E10					Magnetic stripe card T3-
VBUS	C6					USB VBUS
DP	B6					USB DP
DN	B5					USB DN
ID	C5					USB ID
DRV_VBUS	A7	DRV_VBUS	PB[6]	PWM6		
PA4	A1		PA[4]	PWM4	XTAL32K	
PA5	B1		PA[5]	PWM5	CLK_24M	Configurable output 24M
PE[6]	F1	UART3_CTS	PE[6]	I2C0_SCL		
PE[7]	F2	UART3_RTS	PE[7]	I2C0_SDA		
EXT0	E5					External Tamper0
EXT1	F5					External Tamper1
EXT2	G5					External Tamper2
EXT3	E6					External Tamper3
EXT4	F6					External Tamper4
EXT5	G6					External Tamper5
EXT6	E7					External Tamper6
EXT7	F7					External Tamper7
XO32	A4					XTAL 32K Output
XI32	B4					XTAL 32K Input

XO12M	A8					XTAL 12M Output
XI12M	B8					XTAL 12M Input
RSTN	J9					Reset Pin
VDD33	D2					
VDD33	L2					
VDD33	J10					
VDD33	A5					
IO_VCC	L9					PB12~PB15 Pin power input
VDD25	A11					1uF ground capacitance
VDD12	A6					1uF ground capacitance
REFP	A10					1uF ground capacitance
VBAT33	A2					Battery power supply
VSS	B3					
VSS	F3					
VSS	K3					
VSS	K9					
VSS	F9					
VSS	B9					

2.3 Package Information

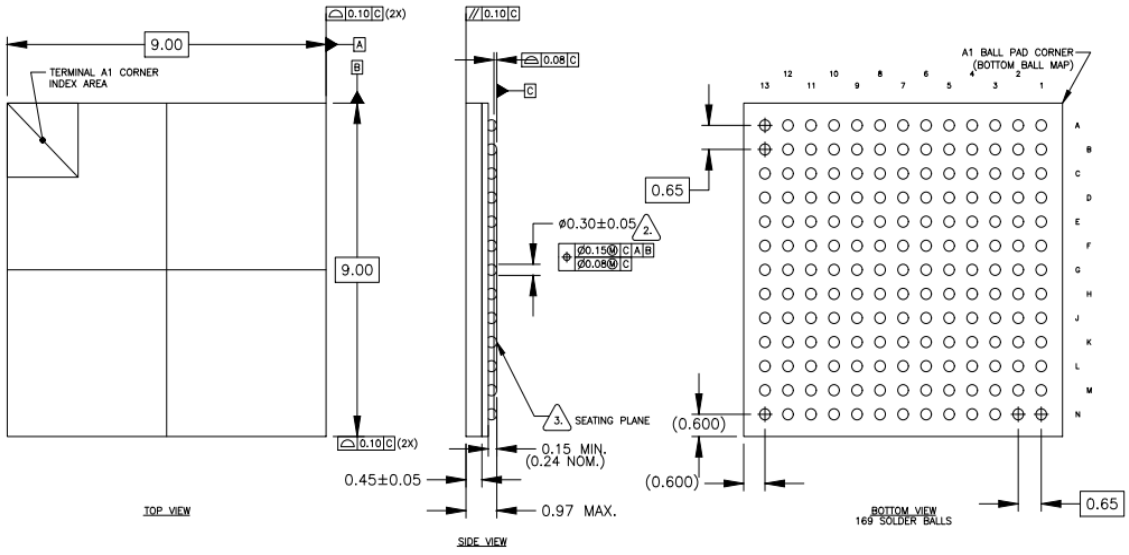

Figure 2 MH1903 BGA169 9mm × 9mm Package Size

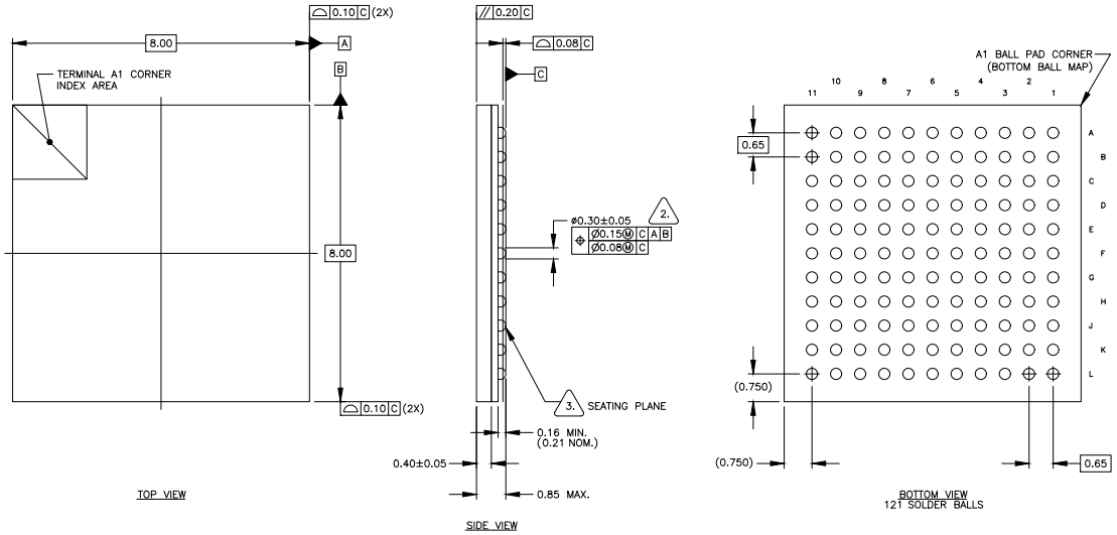

Figure 3 MH1903 BGA121 8mm × 8mm Package Size

3 Chip Function Module

3.1 Peripheral Description

3.1.1 SPI

Chip provides 4 SPI master / slave,1 SPI master device interfaces, it can support to communicate with multiple slaves when as master device interface.

SPI peripheral features:

- Master mode and Slave mode independent address operation
- Master mode supports full duplex, Simplex receive, simplex send, EEPROM mode
- Multiple Master Conflict detection
- Supports Motorola SPI, Texas Instruments SPI, National Semiconductor Microwire three communication modes
- Independent receive and send FIFO, receive and send FIFO depth are 16, the width is fixed to 16bits
- frame length can be configured, the range of 4-16bits
- DMA interface

Common Motorola SPI communication protocol supports four communication modes, can achieve full-duplex communication. The system defaults to mode 0 work mode when the system is power on.

SPI protocol defines 4 kinds of communication mode:

- Mode 0: Clock Polarity (CPOL)=0, Clock Phase(CPHA) =0. In this mode, the free state of serial synchronous clock is low. The chip samples data on the clock's first rising edge. This mode is default mode;
- Mode 1: Clock Polarity（CPOL）=0，Clock Phase（CPHA）=1. In this mode, the free state of serial synchronous clock is low. The chip samples data on the clock's second falling edge;
- Mode 2: Clock Polarity（CPOL）=1，Clock Phase（CPHA）=0. In this mode, the free state of serial synchronous clock is high. The chip samples data on the clock's first falling edge;
- Mode3: Clock Polarity（CPOL）=1，Clock Phase（CPHA）=1. In this mode, the free state of serial synchronous clock is high. The chip samples data on the clock's second rising edge.

Note: To ensure the proper operation of chip SPI, ensure CSN signal line remain high when conducting the mode switching. Meanwhile, in the communication process when the host think that the slave is occurring error, the host can make the slave return normal through pulling the CSN high.

SPI interface description as follows:

- SCK: The clock input pin of SPI, when using the communication rate of 200K, the need for at least 20us delay between bytes;
- CSN: The chip selects signal of SPI, the input pin of the chip, low is effective;
- MOSI: The data input pin of SPI;
- MISO: The data output pin of SPI.

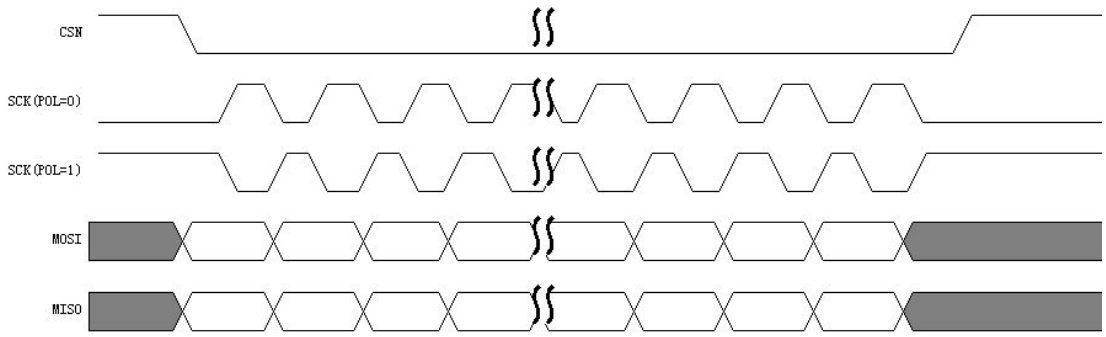

Figure 3 SPI Timing 1 (CPHA=0)

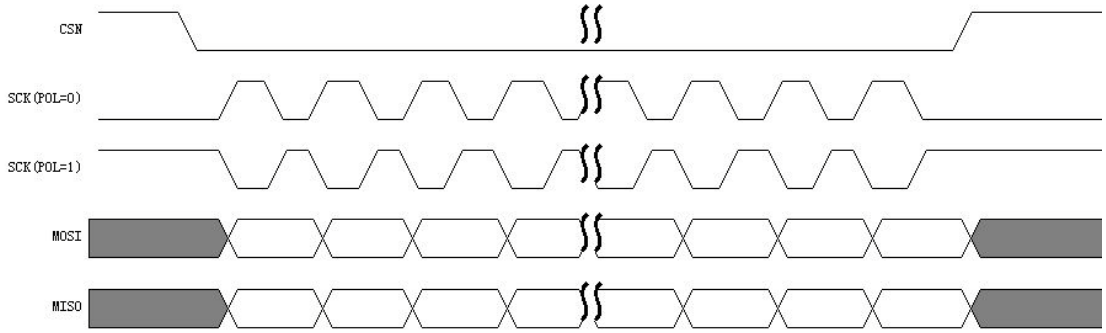

Figure 4 SPI Timing 2 (CPHA=1)

3.1.2 UART

The chip has four full-duplex UART serial communication interfaces, all of which support 4-wire mode.

UART Peripheral Properties:

- Independent receive transmit FIFO, receive send FIFO depth is 16 bytes

  FIFO enable control
- Data bit setting, support for 5-8bit
- Forced 9bit parity bit outpu
- Frame error, check error, break interrupt detection
- IrDA 1.0 infrared protocol support
- DMA reception

The UART peripheral supports independent transmit and receive FIFOs. The FIFO function can be used by configureing the enable bit.

The UART receive and transmit FIFOs support respectively the receive FIFO full and transmit FIFO empty interrupts, and their trigger values are configurable. The transmit FIFO interrupt sources share the same interrupt source with the Transmit Holding Register Empty (THRE) in non-FIFO mode, and is set by software.

3.1.3 I2C

The chip provides one I2C master / slave interface. As a master device interface, it can support communication with multiple slave devices.

I2C Peripheral Features:

- I2C master and slave mode selection
- 7-bit/10-bit mode support
- Speed support Standard mode and Fast mode
- independent receive and send FIFO, receive and send FIFO depth are 8 bytes
- SDA setup and hold time adjustable
- Multi - host bus arbitration detection
- Support for active termination of transmission
- Glitch Filter Setting (Fast Mode)
- DMA support

3.1.4 SCI

The chip contains two Smart Card Interfaces, which supports the ISO7816-3 standard and the EMV Level-1 specification.

- Support asynchronous T = 0 and T = 1 transmission protocol
- Protocol timing and time parameters can be configured
- 8-character depth to receive, transmit buffer
- Receive, transmit FIFO monitoring interrupt
- Interrupt status register
- When detecting the card is removed, the hardware deactivation timing is automatically triggered
- Deactivation timing can be configured software
- Limited support for synchronization cards (control input and output through registers)

SCI module provides external clock F = PCLK / 2 (SCICLKICC +1), SCICLKICC bit width is 8bit, the range is 0 to 255.

3.1.5 USB

OTG_FS controller interface, in line with USB 2.0 standard and OTG 1.0a specification

● Support USB2.0

● Support OTG1.0a

▪ The identification (ID) of the inserted Class A-B equipment

▪ Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)

▪ In OTG applications, allow the host to turn off VBUS to conserve power

● USB full / low speed device supporting SRP protocol (Class B device)

▪ USB full / low speed device supporting SRP protocol (Class A device)

▪ USB OTG full speed / low speed dual role device

● 512 bytes of dedicated RAM and advanced FIFO management

▪ Configuration different RAM area for different FIFO by software, in order to flexible and effective use of RAM

▪ Each FIFO can store multiple data packets

▪ Allows dynamic allocation of memory

▪ Without limiting the length of the FIFO (do not force the length of 2 power, you can use the memory area)

▪ Allow the same endpoint number (IN / OUT endpoint share the same FIFO, more efficient use of storage area)

● Maximum data throughput of one frame (1 ms) is guaranteed without system intervention

● Have a dedicated DMA channel and a proprietary interrupt vector, can speed up data communication speed

● Host mode

▪ Support up to 8 host channels, each channel can be dynamically configured for any type of transmission

▪ Support up to eight interrupts and isochronous transfer requests in a periodic hardware transfer request queue

▪ Supports up to eight transmission requests for control and bulk transfers in non-periodic hardware transfer request queues

3.1.6 BPU & Sensor

The chip built-in BPU module provides BPK unit, Sensor unit and RTC unit.

BPK unit can be powered by the battery power domain, the key is not lost when the external power supply is power down. The BPK register is cleared when the Sensor unit detects an attack.

Sensor features:

● External attack is programmable, support external static and external dynamic modes, external static can program up to 8 detection sources, external dynamic can programming up to 4 pairs of detection sources.

● Internal attack detection includes 32K clock frequency detection, 12M clock frequency detection, high and low temperature attack detection, high and low voltage attack detection.

● Active shelding.

● Battery voltage glitch detection.

3.1.7 GPIO

MH1903 supports up to 128 GPIO, each IO pins are multiplexed with peripherals. Each GPIO can be configured as input, output, interrupt mode, when as an output, the output value of each IO can be configured separately. IO supports strong push-pull output / open-drain output mode.

3.1.8 True Random Numbers

Chip built-in ture random number generator, the user can take up to 128bit true random number.

3.1.9 LCD Controller Interface (LCDI)

This module is used to connect the "LCD display module" (LCD Module), off the chip to communicate with the 8080 or 6800 interface of the "LCD display module".

Main features:

● Supporting 8080 and 6800 4/8-bit interfaces, 4bit mode will execute 4-bit read / write timing twice in a row;

● The clock of interface 8080 or 6800 can be matched;

● The effective levels of each signal at the interface of 8080 or 6800 are configurable;

● The interface driving mode is divided into "automatic mode" and "manual mode". "automatic mode" is driven by LCDI to drive each port signal, and "manual mode" is equivalent to GPIO;.

● The TX/RX interrupt can be produced, and the interrupt can be matched.

3.1.10 Keyboard Control Unit (KCU)

The keyboard control unit is used for scanning and identifying keyboard keys and has the security feature of resisting electromagnetic attack.

Main features:

● The maximum can provide 4x5 array, 20 keys;

● The key can be configured to shake the (Debounce) time;

● More than 4 keystroke cache registers;

● Press the key to press the (Push) and the button to release the (release) probe;

● Random keyboard scanning against electromagnetic attack;

● The port of the keyboard array is built-in pull-up in the chip IO;

● Multiple keys are not supported to be pressed at the same time.

3.1.11 DMA Controller (DMAC)

The direct memory access (DMA) is used to provide high-speed data transmission between the peripheral and the memory or between the memory and the memory. Without CPU intervention, data can be moved quickly through DMA, saving CPU resources for other operations.

The DMA controller has eight channels, each dedicated to managing memory-to-memory, memory-to-peripheral, peripheral-to-memory access requests. Each channel has a separate priority setting.

Main features:

● More than 8 separate configurable channels.

● More than 8 standalone hardware DMA requests (DMA hard handshake interface), each channel also supports software departure (DMA soft handshake interface).

● Independent priority setting for more than 8 channels

● Support for multiple width data transmission.

● Each channel has its own independent interrupt signal and mark.

● Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory transfer.

3.1.12 QSPI Controller.

The chip QSPI controller supports standard SPI and Quad SPI communication.

Main features:

● Support for single-line (Single) and four-wire (Quad) I ≈ O commands

● Configurable DMA controller for access

● The command parameters / format, SPI polarity / phase, etc., can be configured and have good compatibility

3.1.13 DCMI Interface

The digital camera interface (DCMI) is a synchronous parallel interface that accepts high-speed data streams from external 8-bit, 10-bit, 12-bit or 14-bit CMOS camera modules. Different data formats can be supported: video and compressed data. The DCMI interface can receive high-speed (reachable 54MB/s) data streams. The interface contains up to 14 data lines and one pixel clock line. The polarity of the pixel clock can be programmed so that data can be captured at the rising and falling edges of the pixel clock.

Functional characteristics:

● Supports 8-bit, 10-bit, 12-bit, or 14-bit parallel interfaces.

● Support for embedded code / external row synchronization and frame synchronization.

● Support for continuous mode or snapshot mode.

● Support for clipping.

● Supports the following data formats 8 / 10 / 12 / 14 bit line-by-line video: monochrome or raw Bayer format

3.1.14 SDRAM Controller

The SDRAM controller includes initialization, read operation, write operation and automatic refresh operation.

Main features:

● Support for read and write operations with Burst length 8

● Support for 16-bit and 32-bit wide SDRAM

● Automatic refresh

● Initialization

● A priority arbitration mechanism between read, write, automatic refresh, and initialization, as well as a conversion mechanism

3.1.15 SDIO Host Interface

The chip supports SDIO Host interface. SDIO card is an interface developed on the basis of SD memory card interface. the SDIO interface is compatible with the previous SD memory card, and can connect to the device with SDIO interface. at present, the device classes supported by SPEC,SDIO interface according to SDIO protocol are Bluetooth and network card. TV cards, etc.

SDIO bus is similar to USB bus. SDIO bus also has two ends, one of which is Host end, and the other end is DEVICE. the design of HOST-DEVICE is to simplify the design of DEVICE, and all the communication is started with the command issued by HOST end. On the device side, as long as the command of HOST is parsed, you can communicate with HOST.

3.1.16 MIPI CSI-2 interface

The chip supports the MIPI CSI-2 interface, which is an upgraded version of the original standard of the MIPI camera interface, with advanced architectural design, providing greater value to developers, manufacturers, and ultimate consumption, while maintaining the advantages of the standard interface. The camera serial interface 2 specification provides higher interface bandwidth and better channel layout flexibility than previous versions.

Main characteristics:

- Serial Interface Specification 2 (CSI-2) for compatible MIPI Consortium cameras.
- Spports up to two data channels and one clock channel.
- Image pixel interface.
- Support for multiple frame formats.
- All primary and secondary data formats.
- Error detection and correction: PHY errors, packet errors, row errors, frame errors, etc.