MEGAHUNT

MH1608
Datasheet

Contactless Reader Chip

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1. Introduction

The MH1608 is a highly integrated, ultra-low power,reader/writer for contactless communication at 13.56 MHz and supports the contactless reader mode in accordance with ISO/IEC 14443 Type A/B.

2. Characteristics

- Compatible with CV520、MFRC522、MFRC523、PN512
- Digital working voltage range is 1.6V ~ 6V, analog working voltage range is 2.0V ~ 6V
- The chip consumes very low power and the effective communication distance is up to 9cm
- Supports ISO/IEC 14443 TypeA protocol
- Supports Apple Pay、Samsung Pay and other mobile payment applications
- Supports ISO/IEC 14443 TypeB protocol
- Supports P2P passive initiator mode of ISO/IEC 18092
- Supports ISO 14443 A high transmission rate communication: 106kbit/s, 212kbit/s, 424kbit/s
- Supports MFIN/MFOUT
- Supported host interfaces：
  - —SPI up to 10 Mbit/s
  - —I2C interface, the standard mode rate is 100kbit/s
  - —Serial UART with transfer rates up to 1228.8kbit/s
- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Programmable timer
- Three power-saving modes: hardware power-down, software power-down, and transmitter power-down
- Built-in temperature sensor to automatically stop RF emission when the chip temperature is too high
- Power supply from multiple separate sets of power supplies to avoid interference between modules and improve the stability of work
- With CRC and parity check function, built-in CRC coprocessor, in line with ISO/1EC14443 and CCITT protocol

- Internal oscillator, connected to 27.12MHz crystal
- Programmable I/O pins
- Support for low power card detection (LPCD) function

3. Working conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVDD	digital supply voltage	PVSS=DVSS=AVSS=TVSS=0V PVDD=DVDD<=AVDD<=TVDD	1.6	3.3	6	V
AVDD	analog supply voltage		2.0	3.3	6	V
TVDD	transmitter power supply voltage					
PVDD	pin supply voltage	PVSS=DVSS=AVSS=TVSS=0V PVDD=DVDD<=AVDD<=TVDD	1.6	3.3	6	V
T_A	operating temperature		-40		+85	℃

[1] PVDD must be equal to DVDD，not less than DVDD

[2] PVDD and DVDD must be less than or equal to AVDD and TVDD

[3] AVDD must be less than or equal to TVDD

[4] Recommended power supply conditions：PVDD=DVDD=AVDD<=TVDD

4. Electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
3.3V electrical characteristics						
I_{HPD}	hard power down current	AVDD=DVDD=TVDD=PVDD=3.3V NRSTPD=LOW	—	0.02	—	uA
I_{SPD}	soft power down current	AVDD=DVDD=TVDD=PVDD=3.3V RF level detector turn on	—	0.5	—	uA
I_{IDLE}	idle current	AVDD=DVDD=TVDD=PVDD=3.3V	—	2.4	—	mA
I_{DVDD}	digital supply current	DVDD=3.3V	—	1.97	—	mA
I_{AVDD}	analog supply current	AVDD=3.3V，Bit RCVOff＝0	—	1.98	—	mA
	analog supply current	AVDD=3.3V，Bit RCVOff＝1	—	1.95	—	mA
I_{TVDD}	transmitter power current	Continuous launch carrier， TVDD=3.3V	—	60	100	mA

V_{Ripple}	anti-power ripple				400	mV
V_{Noise}	anti-power random noise				1600	mV
R_{TX}	TX1/TX2 output resistance			25		Ω
V_{RX}	RX input sensitivity	f_{SUB}=848kHz		0.5		mVrms
R_{Rx}	Rx output resistance			50		KΩ
V_{POR}	power-on reset voltage			1.5		V
T_{OSU}	crystal start-up time			700		us
5V electrical characteristics						
I_{HPD}	hard power down current	AVDD=DVDD=TVDD=PVDD=5V NRSTPD=LOW	—	0.02	—	uA
I_{SPD}	soft power down current	AVDD=DVDD=TVDD=PVDD=5V RF level detector turn on	—	0.6	—	uA
I_{IDLE}	idle current	AVDD=DVDD=TVDD=PVDD=5V	—	2.5	—	mA
I_{DVDD}	digital supply current	DVDD=5V	—	2.2	—	mA
I_{AVDD}	analog supply current	AVDD=5V，Bit RCVOff＝0	—	2.1	—	mA
	analog supply current	AVDD=5V，Bit RCVOff＝1	—	2.07	—	mA
I_{TVDD}	transmitter power current	Continuous launch carrier，TVDD=5V	—	90	180	mA
V_{Ripple}	anti-power ripple				300	mV
V_{Noise}	anti-power random noise				1600	mV
R_{TX}	TX1/TX2 output resistance			20		Ω
V_{RX}	RX input sensitivity	f_{SUB}=848kHz		0.5		mVrms
R_{Rx}	Rx output resistance			50		KΩ
V_{POR}	power-on reset voltage			1.5		V
T_{OSU}	crystal start-up time			700		us

5. Low power application example

Card type	height vs. Operating current						
	1 cm	2 cm	3 cm	4 cm	5 cm	6 cm	7 cm
S50	10 mA	10 mA	12 mA	15 mA	17 mA	21 mA	25 mA
S70	10 mA	10 mA	12 mA	15 mA	17 mA	21 mA	25 mA
Ultra Light	12 mA	12 mA	14 mA	15 mA	21 mA	25 mA	27 mA

Note：

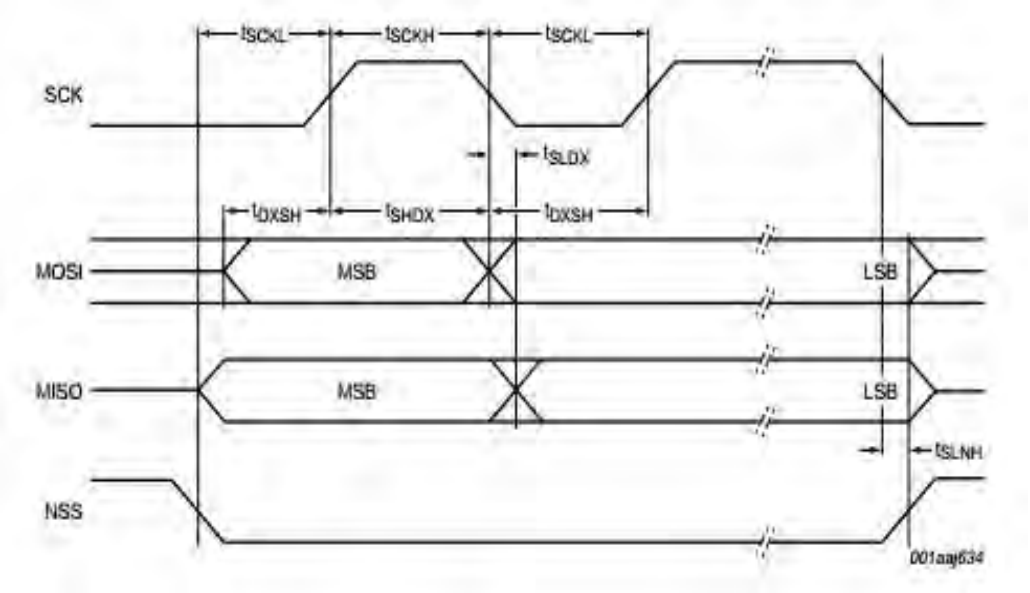
[1] The specific distance of the swipe is affected by antenna size and tuning;

[2] The same distance, different cards due to their different resistance, will cause the introduction of different loads, and then the card reader's current is not the same.

6. SPI timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SCKL}	pulse width LOW	line SCK	50	-	-	ns
t_{SCKH}	pulse width HIGH	line SCK	50	-	-	ns
t_{SHDX}	SCK HIGH to data input hold time	SCK to changing MOSI	25	-	-	ns
t_{DXSH}	data input to SCK HIGH set-up time	changing MOSI to SCK	25	-	-	ns
t_{SLDX}	SCK LOW to data output hold time	SCK to changing MISO	-	-	25	ns
t_{SLNH}	SCK LOW to NSS HIGH time		25	-	-	ns
t_{NHNL}	NSS HIGH time	before communication	50	-	-	ns
t_{DOD}	Data out delay			20		ns
t_{DOHZ}	Data out to high impedance delay			20		ns

SPI timing diagram



Note：

[1] The signal NSS must be LOW to be able to send several bytes in one data stream.

[2] To send more than one data stream NSS must be set HIGH between the data streams.

7. IO electrical characteristics

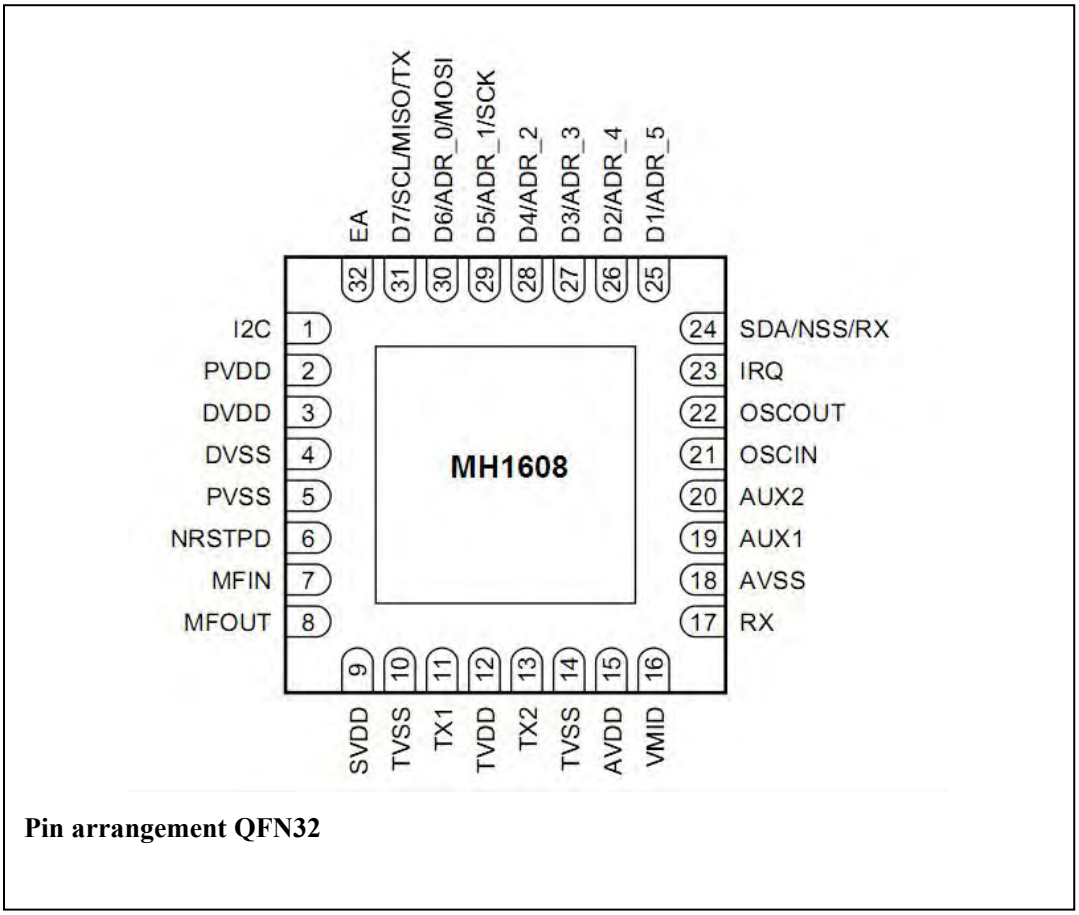
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EA，I2C，NRSTPD						
I_{LEAK}	Input leakage current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
MFIN						
I_{LEAK}	Input leakage current	Work/sleep state pin connection VDD	-1	-	1	uA
		Work/sleep state pin connection GND		14.1		uA
		Work/sleep state pin connection 1.5V		13.1		uA
		Work/sleep state pin suspension		0		uA
V_{IH}	Input voltage high level		0.7PVDD			V

V_{IL}	Input voltage low level				0.3PVDD	V
NSS						
I_{LEAK}	Input leakage current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
OSCIN						
I_{LEAK}	Input leakage current	Work state pin connection VDD		1.1		uA
		Work state pin connection GND		0.6		uA
		Work state pin connection 1.5V		0.4		uA
		Work state pin suspension	-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
D1，D2，D3，D4						
I_{LEAK}	Input leakage current	Work/sleep state pin connection VDD	-1	-	1	uA
		Work/sleep state pin connection GND		13.5		uA
		Work/sleep state pin connection 1.5V		13		uA
		Work/sleep state pin suspension		0		uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V;I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V;I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
I_{OH}	High level output current	VDD(PVDD) = 3 V	-8.5		-7.3	mA
I_{OL}	Low level output current	VDD(PVDD) = 3 V	7.3		8.5	mA

SCK、SDI						
I_{LEAK}	Input leakage current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
SDO						
I_{LEAK}	Input leakage current	Work/sleep state pin connection VDD		13.4		mA
		Work/sleep state pin connection GND	-1	-	1	uA
		Work/sleep state pin connection 1.5V		12.72		mA
		Work/sleep state pin suspension	-1	-	1	uA
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V;I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V;I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
MFOUT、IRQ						
I_{LEAK}	Input leakage current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V;I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V;I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
I_{OH}	High level output current	VDD(PVDD) = 3 V	-8.5		-7.3	mA
I_{OL}	Low level output current	VDD(PVDD) = 3 V	7.3		8.5	mA
OSCOUT						
I_{LEAK}	Input leakage current	Work state pin connection VDD		8.01		mA
		Work state pin connection GND		2.49		mA
		Work state pin connection 1.5V		3.3		mA

		Work state pin suspension	-1	-	1	uA
I_{LEAK}	Input leakage current	Sleep state pin connection VDD		8.35		mA
		Sleep state pin connection GND	-1	-	1	uA
		Sleep state pin connection 1.5V		3.7		mA
		Sleep state pin suspension	-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V;I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V;I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V

8. Pin arrangement

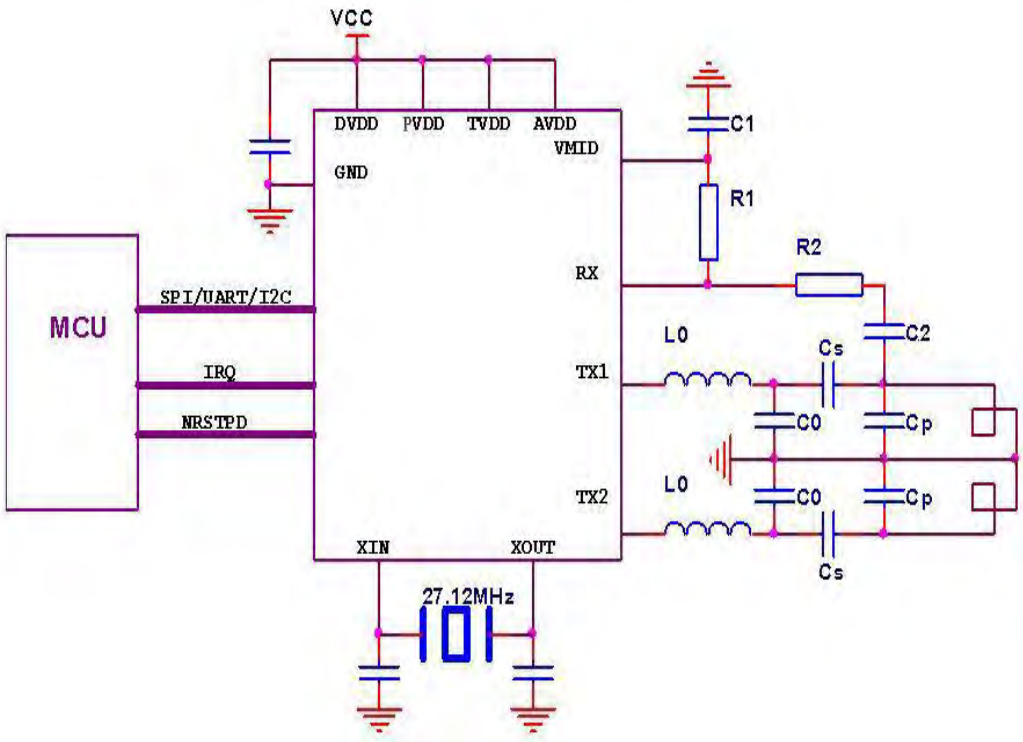


Pin arrangement QFN32

8.1 QFN32 Pin description

序号	符号	类型	描述
1	I2C	I	I2C-bus enable input
2	PVDD	PWR	pin power supply
3	DVDD	PWR	digital power supply
4	DVSS	PWR	digital ground
5	PVSS	PWR	pin power supply ground
6	NRSTPD	I	reset and power-down input: reset: enabled by a positive edge power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world
7	MFIN	I	MIFARE signal input
8	MFOUT	O	MIFARE signal output
9	SVDD	PWR	MFIN and MFOUT pin power supply
10	TVSS	PWR	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	PWR	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	PWR	transmitter output stage 2 ground
15	AVDD	PWR	analog power supply
16	VMID	PWR	internal reference voltage
17	RX	I	RF signal input
18	AVSS	PWR	analog ground
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input; also the input for an externally generated clock (fclk = 27.12 MHz)
22	OSCOUT	O	crystal oscillator inverting amplifier output
23	IRQ	O	interrupt request output: indicates an interrupt event
24	SDA/NSS/RX	I/O	SPI/I2C/UART/Parallel port communication interface
25	D1/ADR_5	I/O	
26	D2/ADR_4	I/O	
27	D3/ADR_3	I/O	
28	D4/ADR_2	I/O	
29	D5/ADR_1/SCK	I/O	
30	D6/ADR_0/MOSI	I/O	
31	D7/SCL/MISO/TX	I/O	
32	EA	I	external address input for coding I2C-bus address

9. Typical application diagram



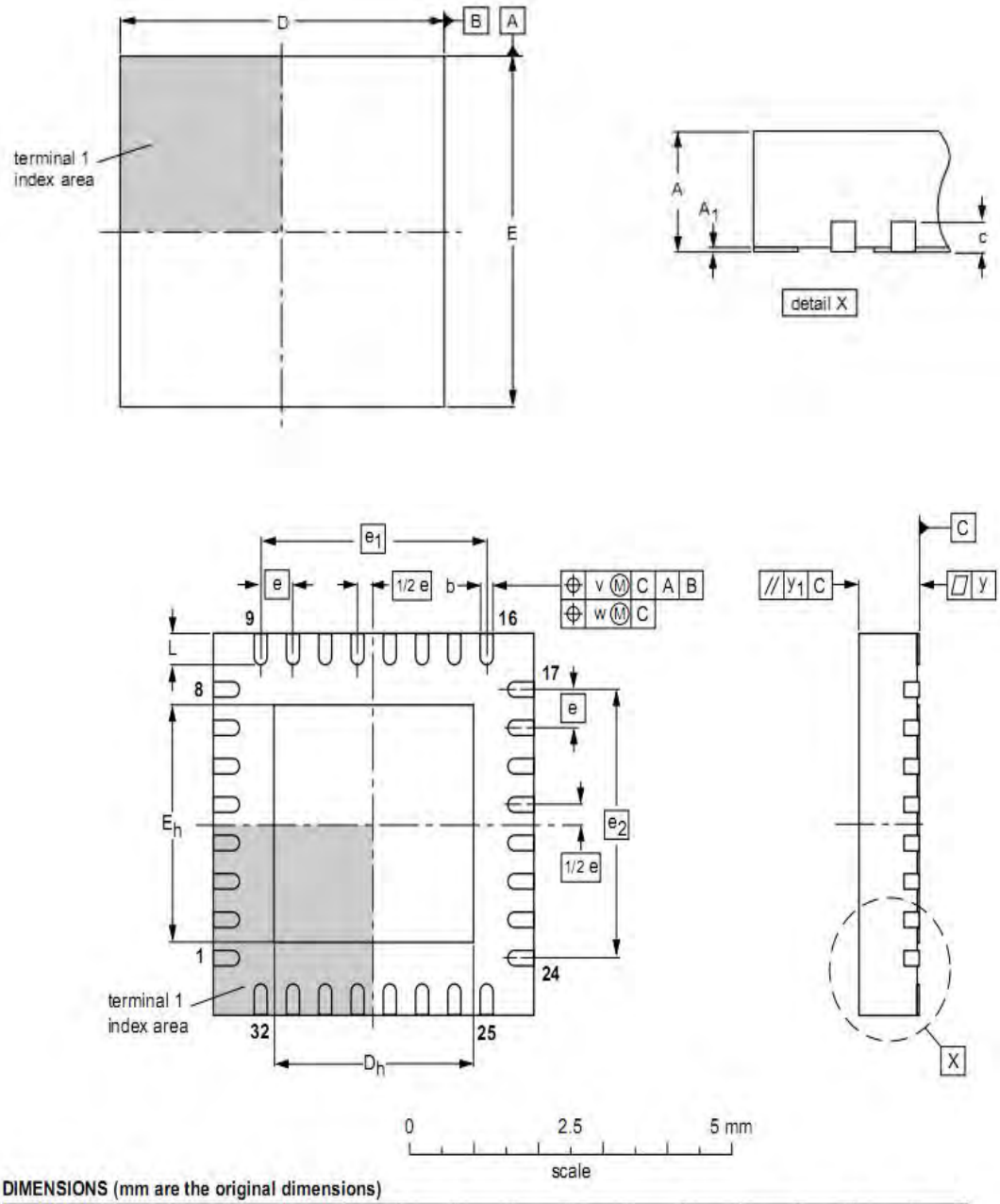
Typical peripheral

Note：

[1] The on-board PCB antenna of this type of circuit needs to be grounded;

[2] This type of circuit supports MIFARE cards with reading and writing distances of up to 9cm, which are affected by antenna size and tuning.

10. Package size



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

QFN32 Package size