

FORESEE®

LPDDR4X/LPDDR4 Datasheet

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LPDDR4X/LPDDR4 Datasheet

IPD1.9.13.3.1-D-0042

FLXC2004G-N1

Version 1.5

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Key Features

Specification Compatibility

- JEDEC Standard No. JESD209-4-1, No. JESD209-4B

Supported Features

- Ultra-low-voltage core and I/O power supplies
 - VDD1 = 1.70–1.95V; 1.80V nominal
 - VDD2 = 1.06–1.17V; 1.10V nominal
 - VDDQ = 1.06–1.17V; 1.10V nominal
 - or VDDQ = 0.57–0.65V; 0.60V nominal
- Frequency range
 - 2133–10 MHz (data rate range: 4266–20 Mbps/pin)
- 16n-prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling

- Up to 17 GB/s per chip (2 channels x 8.5 GB/s)
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable VSSQ (ODT) termination
- Single-ended CK and DQS support

Options

- VDD1/VDD2/VDDQ: 1.80V/1.10V/1.10V or 0.60V
- Array configuration
 - 1Gig x 32 (2 channels x 16 I/O)
- FBGA “green” package
 - 200-ball VFBGA (10mm x 14.5mm x 1.0mm max)
- Speed grade, cycle time
 - 468ps @ RL = 36/40
- Operating temperature range
 - –25°C to +85°C

Table 1 Key Timing Parameters

Clock Rate (MHz)	Data Rate per Pin (Mb/s)	Array Configuration	WRITE Latency		READ Latency	
			Set A	Set B	DBI Disabled	DBI Enabled
2133	4266	1Gig x 32	18	34	36	40

1. Introduction

1.1 General Description

The FORESEE Mobile Low-Power DDR4 SDRAM (LPDDR4X/LPDDR4) is a high-speed CMOS, dynamic random-access memory internally configured with either 1 or 2 channels. Each channel is comprised of 16 DQs and 8 banks.

The LPDDR4X/LPDDR4 uses a 2-tick, single-data-rate (SDR) protocol on the CA bus to reduce the number of input signals in the system. The term "2-tick" means that the command/address is decoded across two transactions, such that half of the command/address is captured with each of two consecutive rising edges of CK. The 6-bit CA bus contains command, address, and bank information. Some commands such as READ, WRITE, MASKED WRITE, and ACTIVATE require two consecutive 2-tick SDR commands to complete the instruction.

The FORESEE LPDDR4X/LPDDR4 uses a double-data-rate (DDR) protocol on the DQ bus to achieve high-speed operation. The DDR interface transfers two data bits to each DQ lane in one clock cycle and is matched to a 16n-prefetch DRAM architecture. A write/read access consists of a single 16n-bit-wide data transfer to/from the DRAM core and 16 corresponding n-bit-wide data transfers at the I/O pins.

1.2 Part Number Decoder

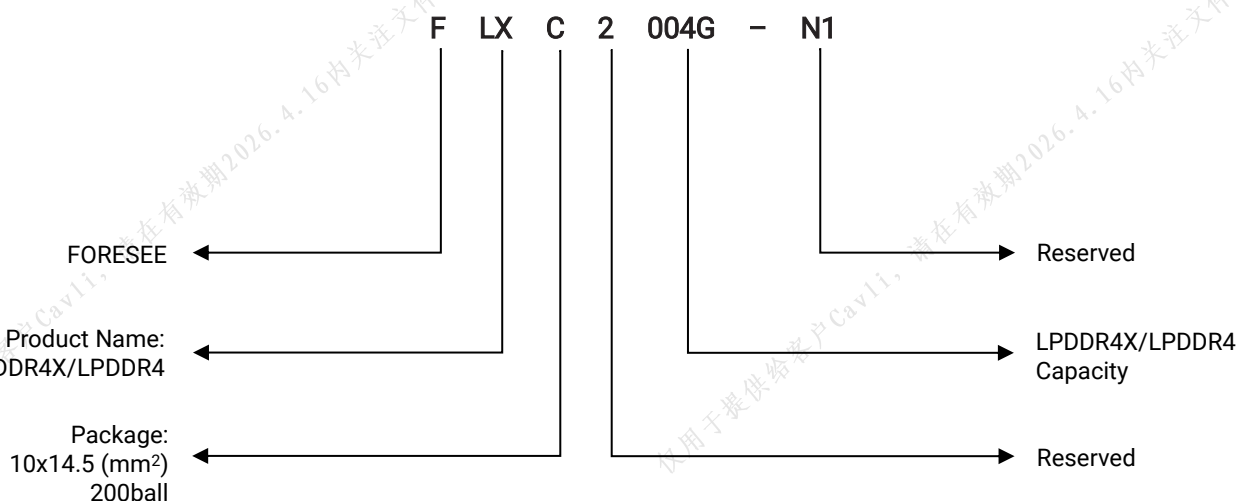


Figure 1 Part Number Decoder

1.3 Ordering Information

Table 2 Ordering Information

Part Number	Package Size (mm)	Memory Combination	Operation Voltage	Density	Speed	Package
FLXC2004G-N1	10*14.5*1.0(max)	LPDDR4/ LPDDR4X	1.80V/1.10V/1.10V or 0.60V	32Gb	4266Mbps	200ball FBGA (Lead & Halogen Free)

2. Product Specifications

2.1 Temperature Specifications

Table 3 Temperature Specifications

The Case Surface Temperature (Tc)	
Operation	-25°C ~ +85°C
Storage	-55°C ~ +125°C

2.2 SDRAM Addressing

Table 4 SDRAM Addressing

Configuration (32Gb/Package)			1Gig x 32
Die Configuration (for package)	Channel A, Rank 0		x16 Mode
	Channel B, Rank 0		x16 Mode
	Channel A, Rank 1		x16 Mode
	Channel B, Rank 1		x16 Mode
Die Addressing	Bank address		BA[2:0]
	x 16	Row address	R[15:0]
		Column address	C[9:0]

2.3 Mode Registers

Table 5 MR5 Basic Configuration 1 (MA[5:0] = 05h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

Table 6 MR5 Op-Code Bit Definitions

Feature	Type	OP	Definition
Manufacturer ID	Read-only	OP[7:0]	1111 1111b: Micron

Table 7 MR8 Basic Configuration 4 (MA[5:0] = 08h)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Table 8 MR8 Op-Code Bit Definitions

Feature	Type	OP	Definition
Type	Read-only	OP[1:0]	00b: S16 SDRAM (16n-prefetch)
Density	Read-only	OP[5:2]	0100b: 16Gb dual-channel die/8Gb single channel die
I/O width	Read-only	OP[7:6]	00b: x16/channel

2.4 Functional Block Diagram

Dual-Channel, Package Block Diagram

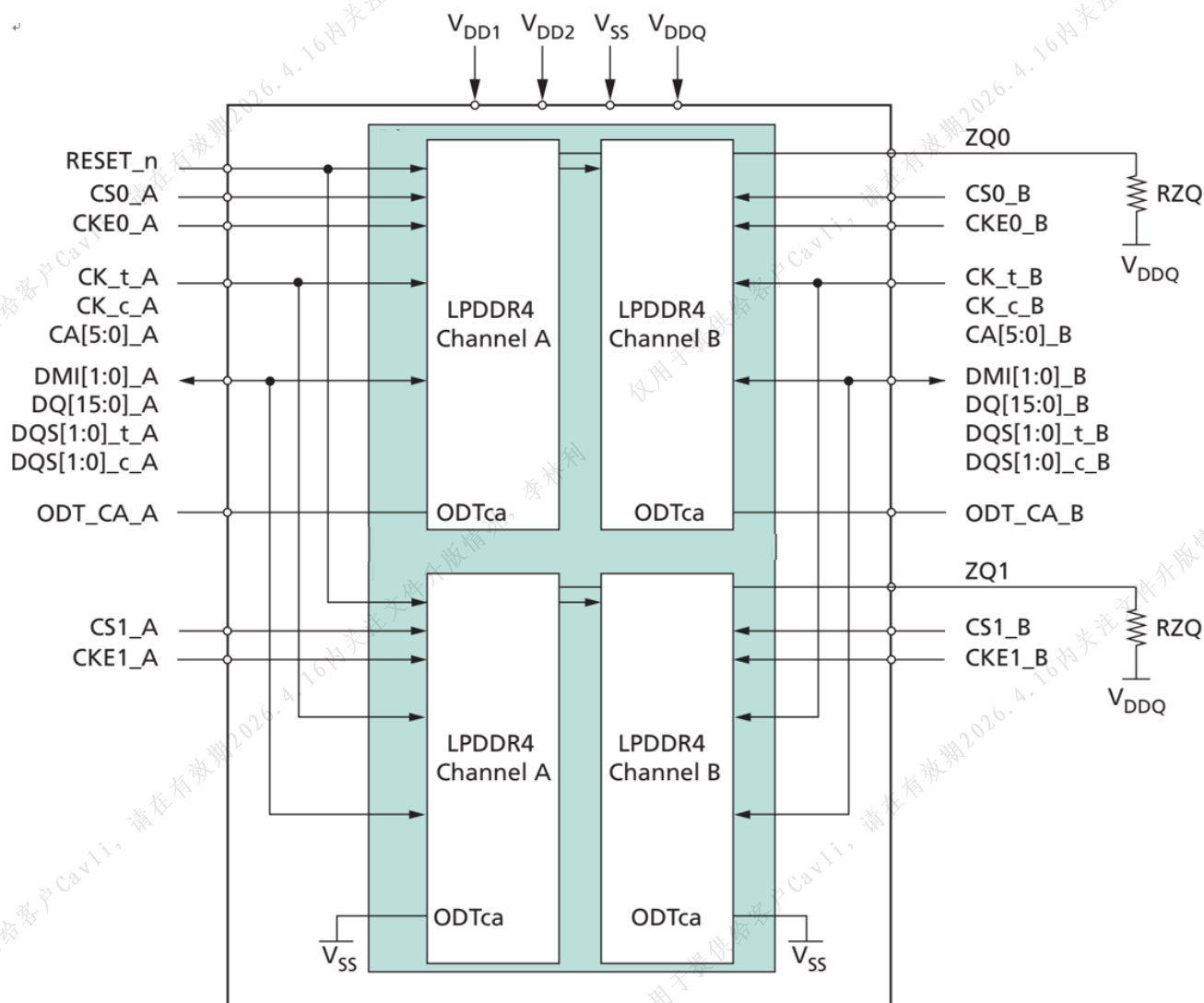


Figure 2 Functional Block Diagram

2.5 Ball Pin Configuration

200-Ball Discrete Dual-Channel VFBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0			ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	DNU
C	VSS	DQ1_A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1_A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_t_A	VSS	VDDQ			VDDQ	VSS	DQS1_t_A	VSS	VDDQ
E	VSS	DQ2_A	DQS0_c_A	DQ5_A	VSS			VSS	DQ13_A	DQS1_c_A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11_A	VDD1
G	VSS	ODT_CA_A	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_A	CS1_A	CS0_A	VDD2			VDD2	CA2_A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	CKE1_B			CK_t_B	CK_c_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	CS1_B	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_CA_B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_c_B	DQ5_B	VSS			VSS	DQ13_B	DQS1_c_B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_t_B	VSS	VDDQ			VDDQ	VSS	DQS1_t_B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	DNU	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	DNU
AB	DNU	DNU	VSS	VDD2	VSS			VSS	VDD2	VSS	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12

Top View

Channel A
 Channel B
 ZQ, ODT_CA, RESET
 Power Supply
 Ground

Figure 3 Ball Assignment

Table 9 Pin Description

Symbol	Type	Description
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A, CKE1_A CKE0_B, CKE1_B	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled on the rising edge of CK.
CS0_A, CS1_A CS0_B, CS1_B	Input	Chip Select: Each rank (0, 1) in each channel (A, B) has its own CS signals.
CA[5:0]_A, CA[5:0]_B	Input	Command/Address Inputs: Provide the command and address inputs according to the Command Truth Table. Each channel (A, B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	CA ODT Control: LPDDR4X: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level. LPDDR4: The ODT_CA pin is used in conjunction with the mode register to turn on/off the on-die termination for CA pins. It is bonded to VDD2 within the package, or at the package ball, for the terminating rank, and the non-terminating ranks are bonded to VSS (or left floating with a weak pull-down on the DRAM die). The terminating rank is the DRAM that terminates the CA bus for all die on the same channel.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data Input/Output: Bidirectional data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data Strobe: DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask/Data Bus Inversion: DMI is a dual-use bidirectional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion(DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command. The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0, ZQ1	Reference	ZQ Calibration Reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to VDDQ through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	Power Supplies: Isolated on the die for improved noise immunity.
VSS	Supply	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET pin resets both channels of the die.
DNU	—	Do Not Use: Must be grounded or left floating.
NC	—	No Connect: Not internally connected.

2.6 Package Dimension

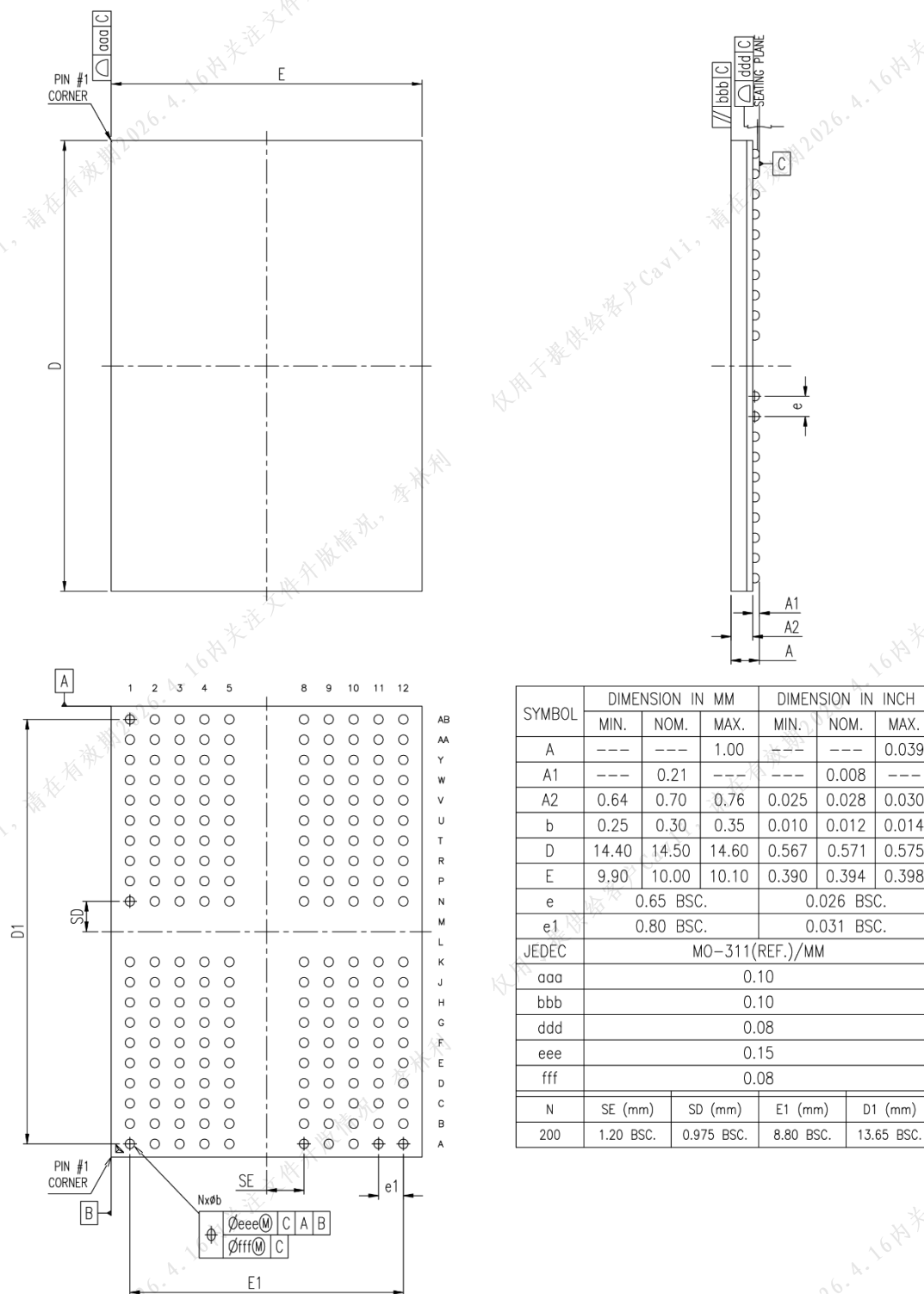


Figure 4 Package Dimension

3. IDD Specification Parameters and Operating Conditions

Table 10 IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: $t_{CK}=t_{CK}(\text{MIN})$; $t_{RC}=t_{RC}(\text{MIN})$; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD01	VDD1	
	IDD02	VDD2	
	IDD0Q	VDDQ	3
Idle power-down standby current: $t_{CK} = t_{CK}(\text{MIN})$; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2P1	VDD1	
	IDD2P2	VDD2	
	IDD2PQ	VDDQ	3
Idle power-down standby current with clock stopped: $CK_t = \text{LOW}$, $CK_c = \text{HIGH}$; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2PS1	VDD1	
	IDD2PS2	VDD2	
	IDD2PSQ	VDDQ	3
Idle non-power-down standby current: $t_{CK} = t_{CK}(\text{MIN})$; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD2N1	VDD1	
	IDD2N2	VDD2	
	IDD2NQ	VDDQ	3
Idle non-power-down standby current with clock stopped: $CK_t = \text{LOW}$; $CK_c = \text{HIGH}$; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD2NS1	VDD1	
	IDD2NS2	VDD2	
	IDD2NSQ	VDDQ	3
Active power-down standby current: $t_{CK} = t_{CK}(\text{MIN})$; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3P1	VDD1	
	IDD3P2	VDD2	
	IDD3PQ	VDDQ	3
Active power-down standby current with clock stopped: $CK_t = \text{LOW}$, $CK_c = \text{HIGH}$; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3PS1	VDD1	
	IDD3PS2	VDD2	
	IDD3PSQ	VDDQ	4
Active non-power-down standby current: $t_{CK} = t_{CK}(\text{MIN})$; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD3N1	VDD1	
	IDD3N2	VDD2	
	IDD3NQ	VDDQ	4
Active non-power-down standby current with clock stopped: $CK_t = \text{LOW}$, $CK_c = \text{HIGH}$; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable; ODT is disabled	IDD3NS1	VDD1	
	IDD3NS2	VDD2	
	IDD3NSQ	VDDQ	4
Operating burst READ current: $t_{CK} = t_{CK}(\text{MIN})$; CS is LOW between valid commands; One bank is active; $BL = 16$ or 32 ; $RL = RL(\text{MIN})$; CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	IDD4R1	VDD1	
	IDD4R2	VDD2	
	IDD4RQ	VDDQ	5
Operating burst WRITE current: $t_{CK} = t_{CK}(\text{MIN})$; CS is LOW between valid commands; One bank is active; $BL = 16$ or 32 ; $WL = WL(\text{MIN})$; CA bus inputs are switching; 50% data change each burst transfer; ODT is disabled	IDD4W1	VDD1	
	IDD4W2	VDD2	
	IDD4WQ	VDDQ	4
All-bank REFRESH burst current: $t_{CK} = t_{CK}(\text{MIN})$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCab}(\text{MIN})$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD51	VDD1	
	IDD52	VDD2	
	IDD5Q	VDDQ	4

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Parameter/Condition	Symbol	Power Supply	Notes
All-bank REFRESH average current: tCK = tCK (MIN); CKE is High between valid commands; tRC = tREFI; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5AB1	VDD1	
	IDD5AB2	VDD2	
	IDD5ABQ	VDDQ	4
Per-bank REFRESH average current: tCK = tCK (MIN); CKE is High between valid commands tRC = tREFI/8; CA bus inputs are switching; Data bus inputs are stable; ODT is disabled	IDD5PB1	VDD1	
	IDD5PB2	VDD2	
	IDD5PBQ	VDDQ	4
Power-down self refresh current(-25°C to +85°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x self refresh rate; ODT is disabled	IDD61	VDD1	6,7,9
	IDD62	VDD2	6,7,9
	IDD6Q	VDDQ	4,6,7,9

Notes:

1. Published IDD values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. IDD current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of VDDQ and VDD2.
5. Guaranteed by design with output load = 5pF and RON = 40 Ω.
6. The 1x Self Refresh Rate is the rate at which the LPDDR4 device is refreshed internally during Self Refresh, before going into the elevated temperature range.
7. This is the general definition that applies to full array Self Refresh.
8. For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
9. IDD6 85 °C is guaranteed, IDD6 45 °C is typical of the distribution of the arithmetic mean.

Table 11 IDD Parameters – Single Die

*VDD2 = 1.06–1.17V; LPDDR4X: VDDQ = 0.57–0.65V; LPDDR4: VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V; TC = –25°C to +85°C

Symbol	Supply	4266Mbps		Unit	Notes
		LPDDR4X	LPDDR4		
IDD01	VDD1	8.00	8.00	mA	
IDD02	VDD2	58.00	58.00		
IDD0Q	VDDQ	1.50	1.50		
IDD2P1	VDD1	2.40	2.40	mA	
IDD2P2	VDD2	3.60	3.60		
IDD2PQ	VDDQ	1.50	1.50		
IDD2PS1	VDD1	2.40	2.40	mA	
IDD2PS2	VDD2	3.60	3.60		
IDD2PSQ	VDDQ	1.50	1.50		
IDD2N1	VDD1	2.40	2.40	mA	
IDD2N2	VDD2	30.00	30.00		
IDD2NQ	VDDQ	1.50	1.50		
IDD2NS1	VDD1	2.40	2.40	mA	
IDD2NS2	VDD2	20.00	20.00		
IDD2NSQ	VDDQ	1.50	1.50		
IDD3P1	VDD1	2.40	2.40	mA	
IDD3P2	VDD2	9.60	9.60		
IDD3PQ	VDDQ	1.50	1.50		

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Symbol	Supply	4266Mbps		Unit	Notes
		LPDDR4X	LPDDR4		
IDD3PS1	VDD1	2.40	2.40	mA	
IDD3PS2	VDD2	9.60	9.60		
IDD3PSQ	VDDQ	1.50	1.50		
IDD3N1	VDD1	3.40	3.40	mA	
IDD3N2	VDD2	42.00	42.00		
IDD3NQ	VDDQ	1.50	1.50		
IDD3NS1	VDD1	3.40	3.40	mA	
IDD3NS2	VDD2	30.00	30.00		
IDD3NSQ	VDDQ	1.50	1.50		
IDD4R1	VDD1	15.00	15.00	mA	2, 3
IDD4R2	VDD2	400.00	400.00		
IDD4RQ	VDDQ	126.10	187.80		
IDD4W1	VDD1	15.00	15.00	mA	2
IDD4W2	VDD2	300.00	300.00		
IDD4WQ	VDDQ	1.50	1.50		
IDD51	VDD1	35.00	35.00	mA	
IDD52	VDD2	190.00	190.00		
IDD5Q	VDDQ	1.50	1.50		
IDD5AB1	VDD1	7.60	7.60	mA	
IDD5AB2	VDD2	36.00	36.00		
IDD5ABQ	VDDQ	1.50	1.50		
IDD5PB1	VDD1	6.00	6.00	mA	
IDD5PB2	VDD2	36.00	36.00		
IDD5PBQ	VDDQ	1.50	1.50		

Notes:

1. Published IDD values except IDD4RQ are the maximum IDD currents considering the worst case conditions of process, temperature and voltage.

2. BL = 16, DBI disabled.

3. IDD4RQ value is for reference only. Typical value. VOH = 0.5 × VDDQ, TC = 25°C.

Table 12 IDD6 Full-Array Self Refresh Current – Single Die

VDD2 = 1.06–1.17V; LPDDR4X: VDDQ = 0.57–0.65V; LPDDR4: VDDQ = 1.06–1.17V; VDD1 = 1.70–1.95V

Temperature	Supply	Full-Array Self Refresh Current (4266Mbps)		Unit
		LPDDR4X	LPDDR4	
25°C	VDD1	0.90	0.90	mA
	VDD2	1.90	1.90	
	VDDQ	0.02	0.02	
85°C	VDD1	5.00	5.00	
	VDD2	12.00	12.00	
	VDDQ	1.50	1.50	

Note:

1. IDD6 25°C is the typical IDD current. IDD6 85°C is the maximum IDD current considering the worst case conditions of process, temperature and voltage.

4. Input / Output Capacitance

Table 13 Input / Output Capacitance

*Notes 1 and 2 apply to the entire table

Parameter	Symbol	Min.	Max.	Unit	Notes
Input capacitance, CK_t and CK_c	CCK	0.5	0.9	pF	
Input capacitance delta, CK_t and CK_c	CDCK	0	0.09		3
Input capacitance, all other input-only pins	CI	0.5	0.9		4
Input capacitance delta, all other input-only pins	CDI	-0.1	0.1		5
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	CIO	0.7	1.3		6
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	0	0.1		7
Input/output capacitance delta, DQ, DMI	CDIO	-0.1	0.1		8
Input/output capacitance, ZQ pin	CZQ	0	5.0		

Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA)), with VDD1, VDD2, VDDQ, VSS, VSS, VSS applied and all other pins floating.
3. Absolute value of CCK_t – CCK_c.
4. CI applies to CS, CKE, and CA [5:0].
5. CDI = CI – 0.5 × (CCK_t + CCK_c); It does not apply to CKE.
6. DM loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. CDIO = CIO – Average (CDQn, CDMI, CDQS_t, CDQS_c) in byte-lane.

5. Absolute Maximum DC Ratings

Stresses greater than those listed in the table below may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these conditions, or any other conditions outside those indicated in the operational sections of this document, is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 14 Absolute Maximum DC Ratings

Parameter	Symbol	Min.	Max.	Unit	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.1	V	1
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.5	V	1
VDDQ supply voltage relative to VSS	VDDQ	-0.4	1.5	V	1
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.5	V	
Storage temperature	TSTG	-55	125	°C	2

Notes:

1. For information about relationships between power supplies, see the Initialization Timing Parameters section.
2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to the JE5D51-2 standard.

6. Recommended DC Operating Conditions

Operation or timing that is not specified is illegal. To ensure proper operation, the device must be initialized properly.

Table 15 Recommended DC Operating Conditions

Symbol	Min.	Typ	Max.	DRAM	Unit	Notes
VDD1	1.70	1.80	1.95	Core 1 power	V	1,2
VDD2	1.06	1.10	1.17	Core 2 power/Input buffer power	V	1,2,3
VDDQ	0.57/1.06	0.60/1.10	0.65/1.17	I/O buffer power	V	2,3

Notes:

1. VDD1 uses significantly less power than VDD2.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. The voltage noise tolerance from DC to 20MHz exceeding a peak-to-peak tolerance of 45mV at the DRAM ball is not included in the TdIVW.

7. Initialization Timing Parameters

Table 16 Initialization Timing Parameters

Parameter	Min.	Max.	Unit	Comment
tINIT0	—	20	ms	Maximum voltage ramp time
tINIT1	200	—	μs	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	—	ns	Minimum CKE LOW time before RESET_n goes HIGH
tINIT3	2	—	ms	Minimum CKE LOW time after RESET_n goes HIGH
tINIT4	5	—	tCK	Minimum stable clock before the first CKE HIGH
tINIT5	2	—	μs	Minimum idle time before the first MRW/MRR command
tCKb	Note 1, 2	Note 1, 2	ns	Clock cycle time during boot

Notes:

1. Minimum tCKb guaranteed by DRAM test is 18ns.
2. The system may boot at a higher frequency than dictated by minimum tCKb. The higher boot frequency is system dependent.

8. Electrical Characteristics and AC Timing

8.1 Core Timing Parameters

Refresh rate is determined by the value in MR4 OP [2:0].

Table 17 Core Timing Parameters

Parameter	Symbol	Min. / Max.	Data Rate (Mbps)				Unit	Notes
			2400	3200	3733	4266		
READ latency (DBI disabled)	RL-A	Min.	24	28	32	36	tCK(AVG)	
READ latency (DBI enabled)	RL-B	Min.	28	32	36	40	tCK(AVG)	
WRITE latency (Set A)	WL-A	Min.	12	14	16	18	tCK(AVG)	
WRITE latency (Set B)	WL-B	Min.	22	26	30	34	tCK(AVG)	
ACTIVATE-to-ACTIVATE command period (the same bank)	tRC	Min.	tRAS + tRPab (with all-bank precharge) tRAS + tRPpb (with per-bank precharge)				ns	
Minimum self refresh time (entry to exit)	tSR	Min.	MAX(15ns, 3nCK)				ns	
Self refresh exit to next valid command delay	tXSR	Min.	MAX(tRFCab + 7.5ns, 2nCK)				ns	
CAS-to-CAS delay	tCCD	Min.	8				tCK(AVG)	
CAS-to-CAS delay masked write	tCCDM W	Min.	32				tCK(AVG)	
Internal READ-to-PRECHARGE command delay	tRTP	Min.	MAX(7.5ns, 8nCK)				ns	
RAS-to-CAS delay	tRCD	Min.	MAX(18ns, 4nCK)				ns	
Row precharge time (single bank)	tRPpb	Min.	MAX(18ns, 3nCK)				ns	
Row precharge time (all banks)	tRPab	Min.	MAX(21ns, 3nCK)				ns	
Row active time	tRAS	Min.	MAX(42ns, 3nCK)				ns	
		Max.	MIN($9 \times tREFI \times \text{Refresh Rate}$, 70.2)				μs	
Write recovery time	tWR	Min.	MAX(18ns, 4nCK)				ns	
Write-to-read delay	tWTR	Min.	MAX(10ns, 8nCK)				ns	
Active bank A to active bank B	tRRD	Min.	MAX(10ns, 4nCK)			MAX(7.5ns, 4nCK)	ns	1
Precharge-to-precharge delay	tPPD	Min.	4				tCK(AVG)	2
Four-bank activate window	tFAW	Min.	40			30	ns	1
Delay from SRE command to CKE input LOW	tESCKE	Min.	MAX(1.75ns, 3nCK)				--	3

Notes:

- 4267 Mb/s timing value is supported at lower data rates if the device is supporting 4266Mb/s speed grade.
- Precharge to precharge timing restriction does not apply to AUTO PRECHARGE commands.
- Delay time has to satisfy both analog time (ns) and clock count (nCK). It means that tESCKE will not expire until CK has toggled through at least three full cycles (3 tCK) and 1.75ns has transpired.

8.2 Refresh Requirement Parameters

Table 18 Refresh Requirement Parameters

Parameter		Symbol	Density (per channel)	Unit
			8Gb	
Refresh window (tREFW): (1 x Refresh)		tREFW	32	ms
Required number of REFRESH commands in tREFW window		R	8192	--
Average refresh interval (1 x Refresh)	REFab	tREFI	3.904	µs
	REFpb	tREFIpb	488	ns
REFRESH cycle time (all banks)		tRFCab	280	ns
REFRESH cycle time (per bank)		tRFCpb	140	ns
Per bank refresh to per bank refresh time (different banks)		tPBR2PBR	90	ns

8.3 Temperature Derating for AC timing

Table 19 Temperature Derating for AC timing

Parameter	Symbol	Min. / Max.	Data Rate (Mbps)				Unit	Notes
			2400	3200	3733	4266		
DQS output access time from CK_t/CK_c(derated)	tDQSCK	Max.	3600				ps	
RAS-to-CAS delay (derated)	tRCD	Min.	tRCD + 1.875				ns	
ACTIVATE-to- ACTIVATE command period (derated)	tRC	Min.	tRC + 3.75				ns	
Row active time (derated)	tRAS	Min.	tRAS + 1.875				ns	
Row precharge time (derated)	tRP	Min.	tRP + 1.875				ns	
Active bank A to active bank B (derated)	tRRD	Min.	tRRD + 1.875				ns	

Note:

1. Timing derating applies for operation above 85 °C.

8.4 Clock Specifications and Timing

The specified clock jitter is a random jitter with Gaussian distribution. Input clocks violating minimum or maximum values may result in device malfunction.

Table 20 Definitions and Calculations

Symbol	Description	Calculation	Notes
tCK(avg) and nCK	The average clock period across any consecutive 200-cycle window. Each clock period is calculated from rising clock edge to rising clock edge. Unit tCK(avg) represents the actual clock average tCK(avg) of the input clock under operation. Unit nCK represents one clock cycle of the input clock, counting from actual clock edge to actual clock edge. tCK(avg) may change no more than ±1% within a 100-clock-cycle window, provided that all jitter and timing specifications are met.	$tCK(avg) = (\sum_{j=1}^N tCKj) / N$ Where N = 200	
tCK(abs)	The absolute clock period, as measured from one rising clock edge to the next consecutive rising clock edge.		1

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Symbol	Description	Calculation	Notes
tCH(avg)	The average HIGH pulse width, as calculated across any 200 consecutive HIGH pulses.	$tCH(avg) = (\sum_{j=1}^N tCHj) / (N \times tCK(avg))$ Where N = 200	
tCL(avg)	The average LOW pulse width, as calculated across any 200 consecutive LOW pulses.	$tCL(avg) = (\sum_{j=1}^N tCLj) / (N \times tCK(avg))$ Where N = 200	
tJIT(per)	The single-period jitter defined as the largest deviation of any signal tCK from tCK(avg).	tJIT(per) = min./max. of (tCKi - tCK(avg)) Where i = 1 to 200	1
tJIT(per),act	The actual clock jitter for a given system.		
tJIT(per),allowed	The specified clock period jitter allowance.		
tJIT(cc)	The absolute difference in clock periods between two consecutive clock cycles. tJIT(cc) defines the cycle-to-cycle jitter.	tJIT(cc) = max. of (tCKi+1 - tCKi)	1
tERR(nper)	The cumulative error across n multiple consecutive cycles from tCK(avg).	$tERR(nper) = (\sum_{j=1}^{i+n-1} tCKj) - (n \times tCK(avg))$	1
tERR(nper),act	The actual clock jitter over n cycles for a given system.		
tERR(nper),allowed	The specified clock jitter allowance over n cycles.		
tERR(nper),min.	The minimum tERR(nper).	$tERR(nper),min. = (1 + 0.68LN(n)) \times tJIT(per),min.$	2
tERR(nper),max.	The maximum tERR(nper).	$tERR(nper),max. = (1 + 0.68LN(n)) \times tJIT(per),max.$	2
tJIT(duty)	Defined with absolute and average specifications for tCH and tCL, respectively	$tJIT(duty),min. = MIN((tCH(abs),min. - tCH(avg),min.), (tCL(abs),min. - tCL(avg),min.)) \times tCK(avg)$ $tJIT(duty),max. = MAX((tCH(abs),max. - tCH(avg),max.), (tCL(abs),max. - tCL(avg),max.)) \times tCK(avg)$	

Notes:

1. Not subject to production testing.
2. Using these equations, tERR(nper) tables can be generated for each tJIT(per), act value.

Table 21 tCK(abs), tCH(abs), and tCL(abs) Definitions

Parameter	Symbol	Minimum	Unit
Absolute clock period	tCK(abs)	tCK(avg),min. + tJIT(per),min.	ps ¹
Absolute clock HIGH pulse width	tCH(abs)	tCH(avg),min. + tJIT(duty),min. ² /tCK(avg),min.	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	tCL(avg),min. + tJIT(duty),min. ² /tCK(avg),min.	tCK(avg)

Notes:

1. tCK(avg),min. is expressed in ps for this table.
2. tJIT(duty),min. is a negative value.

Table 22 Clock AC Timing

Table 22. Clock AC Timing						
Parameter	Symbol	Min. / Max.	Data Rate (Mbps)			Unit
			3200	3733	4266	
Average clock period	tCK(AVG)	Min.	625	535	468	ps
		Max.	100			ns
Average HIGH pulse width	tCH(AVG)	Min.	0.46			tCK(AVG)
		Max.	0.54			

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Data Rate (Mbps) comment

Parameter	Symbol	Min. / Max.	Data Rate (Mbps)			Unit
			3200	3733	4266	
Average LOW pulse width	tCL(AVG)	Min.	0.46			tCK(AVG)
		Max.	0.54			
Absolute clock period	tCK(ABS)	Min.	tCK(AVG)min + tJIT(per)min			ps
Absolute HIGH clock pulse width	tCH(ABS)	Min.	0.43			tCK(AVG)
		Max.	0.57			
Absolute LOW clock pulse width	tCL(ABS)	Min.	0.43			tCK(AVG)
		Max.	0.57			
Clock period jitter	tJIT(per)allowed	Min.	-40	-34	-30	ps
		Max.	40	34	30	
Maximum clock jitter between two consecutive clock cycles (including clock period jitter)	tJIT(cc)allowed	Max.	80	68	60	ps

8.5 CA Rx Voltage and Write Timing

The command and address (CA), including CS input receiver compliance mask for voltage and timing, is shown in the figure 5 below. All CA and CS signals apply the same compliance mask and operate in single data rate mode.

The CA input Rx mask for voltage and timing is applied across all pins, as shown in the figure 6 below. The receiver mask (Rx mask) defines the area that the input signal must not encroach if the DRAM input receiver is expected to successfully capture a valid input signal; it is not the valid data eye.

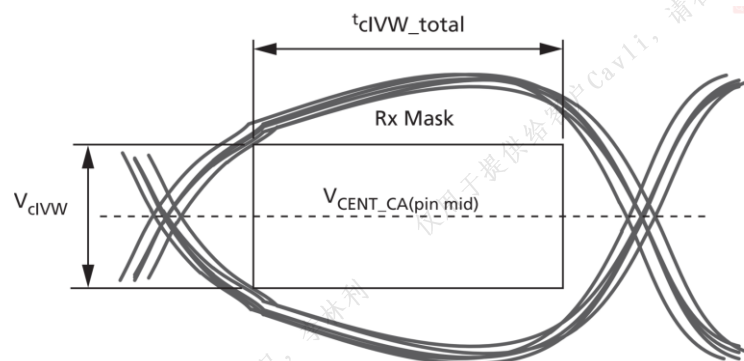


Figure 5 CA Receiver (Rx) Mask

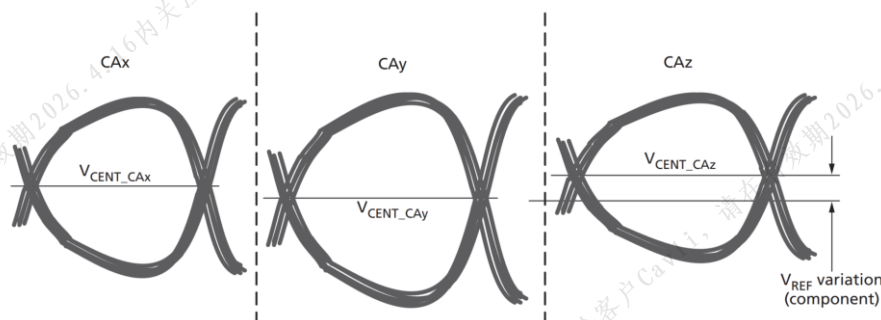


Figure 6 Across Pin VREF (CA) Voltage Variation

VCENT_CA(pin mid) is defined as the midpoint between the largest VCENT_CA voltage level and the smallest VCENT_CA voltage level across all CA and CS pins for a given DRAM component. Each CA VCENT level is defined by the center, which is, the widest opening of the cumulative data input eye, as depicted in the figure 6. This clarifies that any DRAM component level variation must be accounted for within the CA Rx mask. The component-level VREF will be set by the system to account for RON and ODT settings.

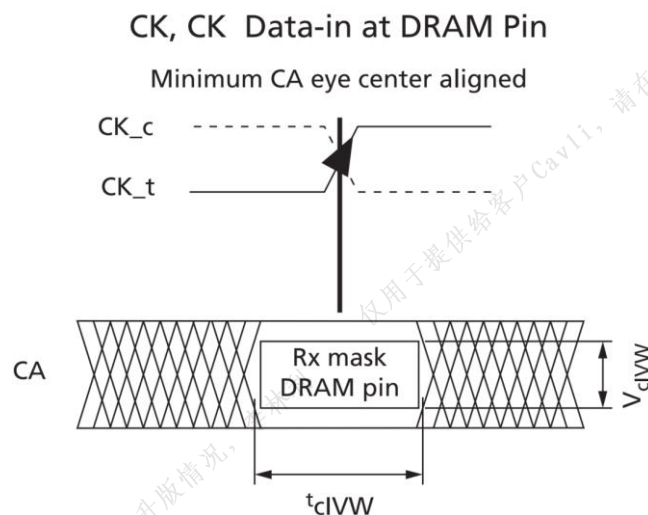


Figure 7 CA Timings at the DRAM Pins

Note:

1. All of the timing terms in the above figure are measured from the CK_t/CK_c to the center (midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around VCENT_CA(pin mid).

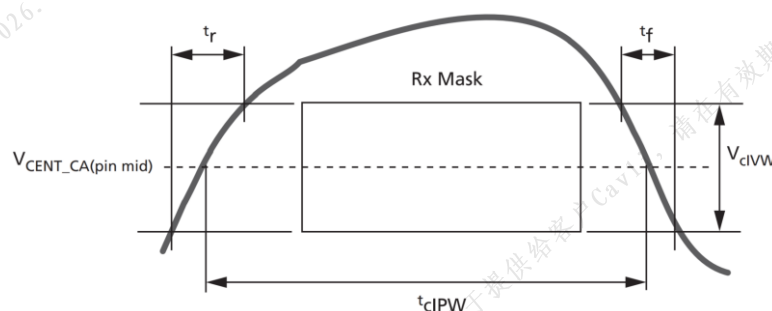


Figure 8 CA t_cIPW and SRIN_cIVW Definition (for Each Input Pulse)

Note:

1. $SRIN_cIVW = V_{dIVW_total} / (t_r \text{ or } t_f)$; signal must be monotonic within t_r and t_f range.

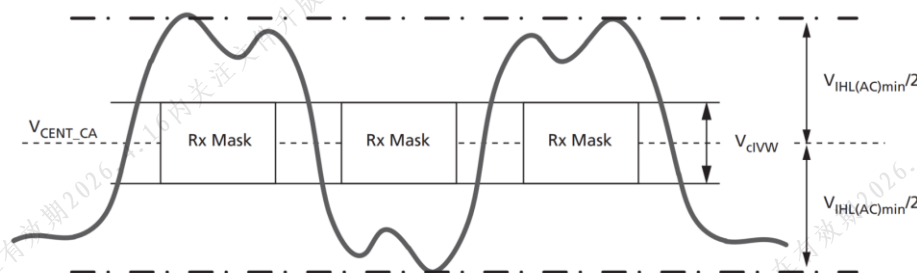


Figure 9 CA VIHL_AC Definition (for Each Input Pulse)

Table 23 DRAM CMD/ADR, CS

*UI = tCK(AVG)MIN

Symbol	Parameter	DQ – 1600/1867		DQ – 3200/3733		DQ – 4266		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
VcIVW	Rx Mask voltage – p-p	--	175	--	155	--	145	mV	1,2,3
TcIVW	Rx timing window		0.3		0.3		0.3	UI	1,2,3
VIHL_AC	CA AC input pulse amplitude pk-pk	210	--	190	--	180	--	mV	4,7
TcIPW	CA input pulse width	0.55	--	0.6	--	0.6	--	UI	5
SRIN_clVW	Input slew rate over VcIVW	1	7	1	7	1	7	V/ns	6

Notes:

1. CA Rx mask voltage and timing parameters at the pin, including voltage and temperature drift.
2. Rx mask voltage VcIVW total(MAX) must be centered around VCENT_CA(pin mid).
3. Vcent_CA must be within the adjustment range of the CA internal Vref.
4. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VcIVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.

8.6 DQ Tx Voltage and Read Timing

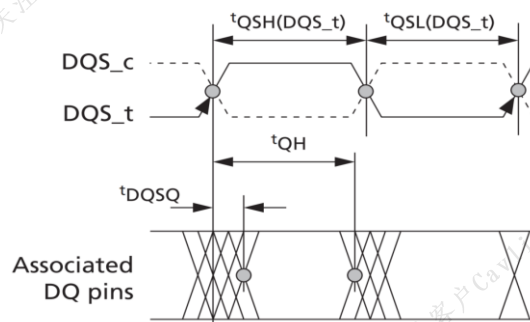


Figure 10 Read Data Timing Definitions – tQH and tDQSQ across DQ Signals per DQS Group

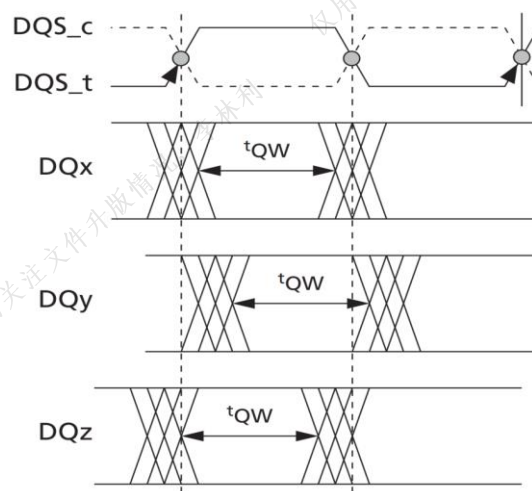


Figure 11 Read Data Timing tQW Valid Window Defined per DQ Signal

Table 24 Read Output Timing

Parameter	Symbol	Min. / Max.	Data Rate (Mbps)			Unit	Notes
			3200	3733	4266		
DQS output access time from CK_t/CK_c	tDQSCK	Min.	1500			ps	1
		Max.	3500				
DQS output access time from CK_t/CK_c – voltage variation	tDQSCK_VOLT	Max.	7			ps/mV	2
DQS output access time from CK_t/CK_c– temperature variation	tDQSCK_TEMP	Max.	4			ps/°s	3
CK to DQS rank to rank variation	tDQSCK_rank2rank	Max.	1.0			ns	4,5
DQS_t, DQS_c to DQ skew total, per group, per access (DBI Disabled)	tDQSQ	Max.	0.18			UI	6
DQ output hold time total from DQS_t, DQS_c (DBI Disabled)	tQH	Min.	MIN(tQSH, tQSL)			ps	6
Data output valid window time total, per pin (DBI-Disabled)	tQW_total	Min.	0.70			UI	6, 11
DQS_t, DQS_c to DQ skew total, per group, per access (DBI-Enabled)	tDQSQ_DBI	Max.	0.18			UI	6
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	Min.	MIN(tQSH_DBI, tQSL_DBI)			ps	6
Data output's valid window time total, per pin (DBI-Enabled)	tQW_total_DBI	Min.	0.70			UI	6, 11
DQS_t, DQS_c differential output's LOW time (DBI-Disabled)	tQSL	Min.	tCL(ABS) – 0.05			tCK(AVG)	9, 11
DQS_t, DQS_c differential output's HIGH time (DBI-Disabled)	tQSH	Min.	tCH(ABS) – 0.05			tCK(AVG)	10, 11
DQS_t, DQS_c differential output's LOW time (DBI-Enabled)	tQSL-DBI	Min.	tCL(ABS) – 0.045			tCK(AVG)	9, 11
DQS_t, DQS_c differential output's HIGH time (DBI-Enabled)	tQSH-DBI	Min.	tCH(ABS) – 0.045			tCK(AVG)	10, 11
Read preamble	tRPRE	Min.	1.8			tCK(AVG)	
Read postamble	tRPST	Min.	0.4 (or 1.4 if extra postamble is programmed in MR)			tCK(AVG)	
DQS Low-Z from clock	tLZ(DQS)	Min.	(RL x tCK)+ tDQSCK(Min) – (tRPRE(Max) x tCK) – 200ps			ps	
DQS Low-Z from clock	tLZ(DQ)	Min.	(RL x tCK) + tDQSCK(Min) – 200ps			ps	
DQS High-Z from clock	tHZ(DQS)	Max.	(RL x tCK) + tDQSCK(Max)+(BL/2 x tCK) + (tRPST(Max) x tCK) – 100ps			ps	
DQHigh-Z from clock	tHZ(DQ)	Max.	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK) -100ps			ps	

Notes:

1. This parameter includes DRAM process, voltage, and temperature variation. It also includes the AC noise impact for frequencies >20 MHz and a max voltage of 45mV peak-to-peak from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply with the component MIN/MAX DC operating conditions.
2. tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. The voltage supply noise must comply with the component MIN/MAX DC operating conditions. The voltage variation is defined as the $\text{MAX}[ABS(tDQSCK(MIN)@V1 - tDQSCK(MAX)@V2), ABS(tDQSCK(MAX)@V1 - tDQSCK(MIN)@V2)]/ABS(V1 - V2)$.

3. tDQSCK_temp MAX delay variation as a function of temperature.
4. The same voltage and temperature are applied to tDQSCK_rank2rank.
5. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design die.
6. DQ-to-DQS differential jitter where the total includes the sum of deterministic and random timing terms for a specified BER.
7. The deterministic component of the total timing.
8. This parameter will be characterized and guaranteed by design.
9. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
10. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from one falling edge to the next consecutive rising edge.
11. This parameter is a function of input clock jitter. These values assume MIN tCH(ABS) and tCL(ABS). When the input clock jitter MIN tCH(ABS) and tCL(ABS) is 0.44 or greater than tCK(AVG), the minimum value of tQSL will be tCL(ABS) - 0.04 and tQSH will be tCH(ABS) - 0.04.

8.7 DQ Rx Voltage and Write Timing

The DQ input receiver mask for voltage and timing is applied per pin, as shown in the figure 12 below. The total mask (VdIVW_total, TdIVW_total) defines the area that the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal. The mask is a receiver property, and it is not the valid data eye.

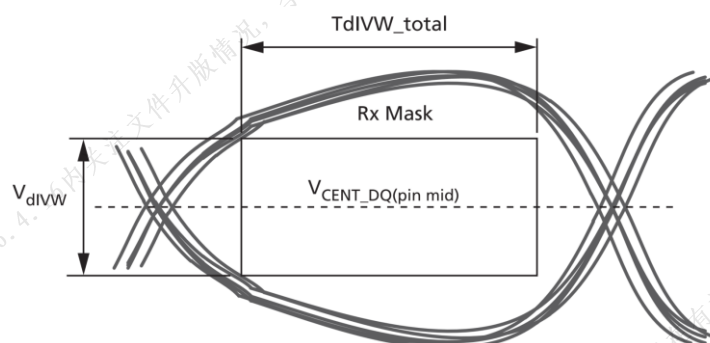


Figure 12 DQ Receiver (Rx) Mask

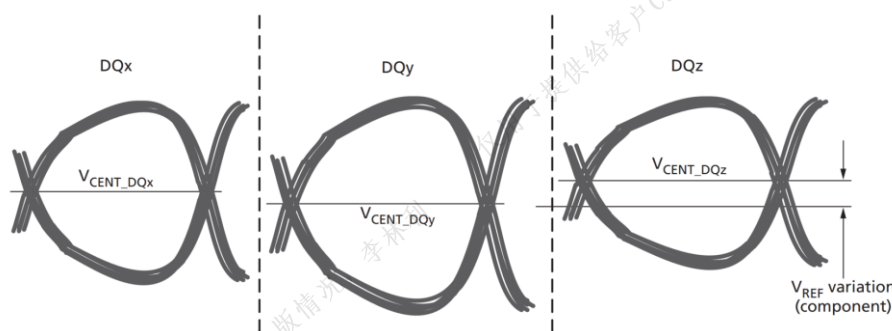
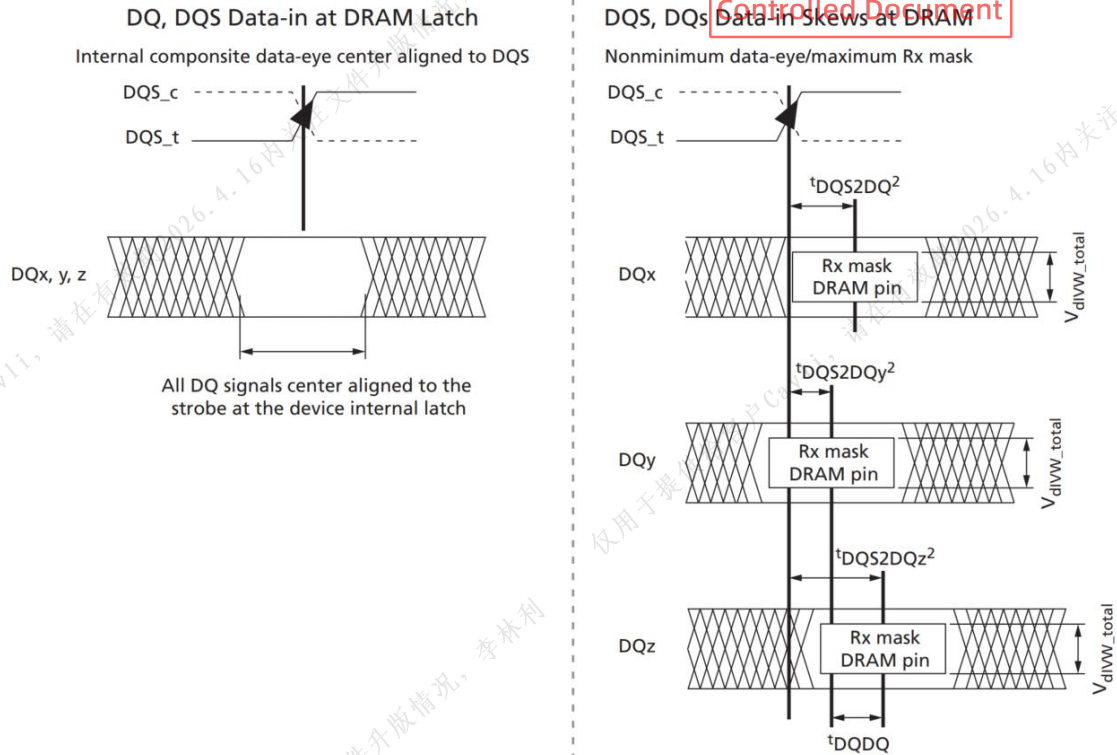


Figure 13 Across Pin VREF DQ Voltage Variation

V_CENT_DQ(pin_mid) is defined as the midpoint between the largest V_CENT_DQ voltage level and the smallest V_CENT_DQ voltage level across all DQ pins for a given DRAM component. Each V_CENT_DQ is defined by the center, which is the widest opening of the cumulative data input eye as shown in the figure 13 above. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level VREF will be set by the system to account for RON and ODT settings.

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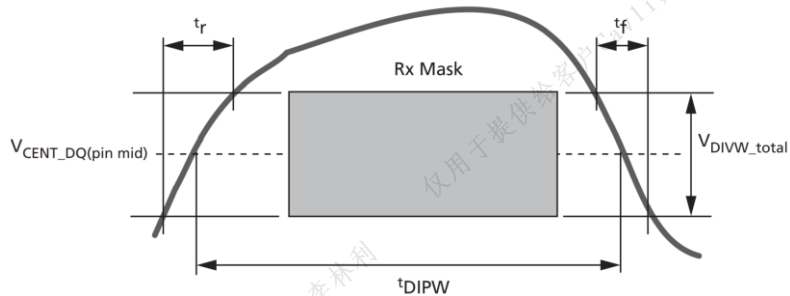
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Figure 14 DQ-to-DQS t_{DQS2DQ} and T_{dqdq}

Notes:

1. These timings at the DRAM pins are referenced from the internal latch.
2. t_{DQS2DQ} is measured at the center (midpoint) of the T_{dIVW} window.
3. DQz represents the MAX t_{DQS2DQ} in this example.
4. DQy represents the MIN t_{DQS2DQ} in this example.

$$UI = t_{CK(AVG)} \text{ MIN}/2$$

Figure 15 DQ t_{DIPW} and $SRIN_dIVW$ Definition (for Each Input Pulse)

Note:

1. $SRIN_dIVW = V_{dIVW_total}/(tr \text{ or } tf)$ signal must be monotonic within tr and tf range.

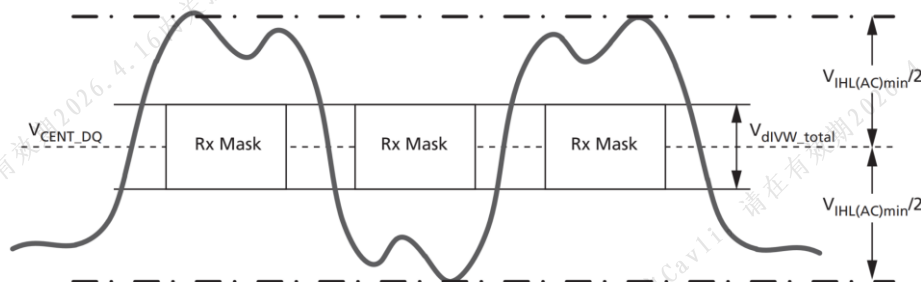
Figure 16 DQ $V_{IH(AC)}$ Definition (for Each Input Pulse)

Table 25 DQs In Receive Mode

*UI = tCK(AVG)(MIN)/2

Symbol	Parameter	2133/2400		3200/3733		4266		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
VdIVW_total	Rx Mask voltage – p-p total	--	140	--	140	--	120	mV	1,2,3,4
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	--	0.22	--	0.25	--	0.25	UI	1,2,4
VIHL_(AC)	DQ AC input pulse amplitude pk-pk	180	--	180	--	170	--	mV	5,13
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45	--	0.45	--	0.45	--	UI	6
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	ps	7
tDQ2DQ	DQ to DQ offset	--	30	--	30	--	30	ps	8
tDQS2DQ_ temp	DQ to DQS offset temperature variation	--	0.6	--	0.6	--	0.6	ps/°C	9
tDQS2DQ_ volt	DQ to DQS offset voltage variation	--	33	--	33	--	33	ps/50 mV	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	V/ns	11
tDQS2DQ_rank 2rank	DQ to DQS offset rank to rank variation	--	200	--	200	--	200	ps	14,15, 16

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and include the DRAM DQ-to-DQS voltage AC noise impact for frequencies >20 MHz with a maximum voltage of 45mV peak-to-peak at a fixed temperature on the package. The voltage supply noise must comply to the component MIN/MAX DC operating conditions.
2. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
6. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
8. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9. TDQS2DQ max delay variation as a function of temperature.
10. TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement VDDQ = VDD2 is assumed.
11. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
12. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13. VIHL_AC does not have to be met when no transitions are occurring.
14. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
15. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
16. tDQS2DQ_rank2rank support was added to JESD209-4B, some older devices designed to support JESD209-4 and JESD209-4A may not support this parameter.

受控文件

Controlled Document

Revision History

Version	Date	Description
1.0	2021/4/20	Initial Release
1.1	2023/2/9	Updated Template
1.2	2023/10/25	Updated IDD Parameters
1.3	2024/4/15	Update Refresh Parameters
1.4	2024/10/10	Update the Frequency
1.5	2025/11/4	Update several IDD parameters