MEGAHUNT

MH1610
Brief Introduction

Contactless Reader Chip

Version: 1.1
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Megahunt Tehnologies Inc.

Revision Record

Date	Revised version	Description	Author
January 4, 2020	V1.0	Complete document	YYGJ
February 4, 2020	V1.1	Emphasis of isolation of power supply and ground	YYGJ

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Overview

MH1610 is a high-performance NFC & EMVCo reader chip with high integration level and low power consumption, which works under the frequency of 13.56MHz and supports contactless reader mode complying with ISO/IEC 14443 TypeA/B protocol.

Features

- Wide digital operating range: 1.6V-6V; Wide analog operating range: 2.0V-6V
- Support EMV3.0 certification, including electric, protocol and phone compatibility certification test
- The power consumption of chip is low; the effective communication distance can reach 9cm
- Support ISO/IEC 14443 Type A protocol
- Support Apple Pay, Samsung Pay and other mobile payment applications
- Support ISO/IEC 14443 Type B protocol
- Support P2P passive initiator mode of ISO/IEC 18092
- Support communication of ISO 14443 A with high transmission rate: 106kbit/s, 212kbit/s and 424kbit/s
- Support MFIN/MFOUT
- Supported host interface:

  －10Mbit/s SPI interface

  －I2C interface, with the rate of 100kbit/s under standard mode

  －Serial UART, transmission rate up to 1228.8kbit/s
- 64 bytes sending and reception of FIFO buffer zone
- Flexible interruption mode
- Programmable timer
- With three power-saving modes: hardware power-down, software power-down and transmitter power-down
- With built-in temperature sensor, to facilitate the automatic stop of RF emission in case of

excessive high chip temperature

- Adopt several groups of power supplies that are mutually independent for supplying power, to avoid the mutual interference between modules and improve the stability of the work
- With CRC and parity check function, with built-in CRC coprocessor, which complies with ISO/1EC14443 and CCITT protocol
- Internal oscillator, connected to 27.12MHz crystal
- With self-owned programmable I/O pin
- Support the function of low-power consumption detection (LPCD)

Operating conditions

Symbol	Parameters	Condition	Min	Typ	Max	Unit
DVDD	Digital power voltage	VSS=TVSS=AVSS=GND=0V DVDD<=SVDD<=AVDD<=TVDD	1.6	3.3	6	V
AVDD	Analog power voltage		2.0	3.3	6	V
SVDD	Analog power voltage					
TVDD	Transmitter power voltage					
TA	Working temperature		-40		+85	℃

[1] SVDD and DVDD must be less than or equal to AVDD and TVDD

[2] AVDD must be less than or equal to TVDD

[3] Recommended power supply conditions: SVDD=DVDD=AVDD<=TVDD

Electrical characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
3.3V electrical characteristics						
I_{HPD}	Hard power-down current	AVDD=DVDD=TVDD=PVDD=3.3V NRSTPD=LOW	—	0.02	—	uA
I_{SPD}	Soft power-off current	AVDD=DVDD=TVDD=PVDD=3.3V Opening of RF level detector	—	1.5	—	uA
I_{IDLE}	Idle current	AVDD=DVDD=TVDD=PVDD=3.3V	—	2.5	—	mA
I_{DVDD}	Digital power current	DVDD=3.3V	—	1.97	—	mA
I_{AVDD}	Analog power current	AVDD=3.3V, in case of RCVOff＝0	—	1.98	—	mA
	Analog power current	AVDD=3.3V, in case of RCVOff＝1	—	1.95	—	mA
I_{TVDD}	Transmitter power current	Continuous emission of carrier, TVDD=3.3V	—	100	170	mA
V_{Ripple}	Power ripple resistance				400	mV
V_{Noise}	Anti-power random noise				1600	mV
R_{TX}	TX1/TX2 output resistance			25		Ω
V_{RX}	RX input sensitivity	f_{SUB}=848kHz		0.5		mVrms
R_{Rx}	Rx input resistance			50		KΩ
V_{POR}	Power-on resetting voltage			1.5		V
T_{OSU}	Starting time of crystal oscillator			300		us
5V electrical characteristics						
I_{HPD}	Hard power-down current	AVDD=DVDD=TVDD=PVDD=5V	—	0.02	—	uA

		NRSTPD=LOW				
I_{SPD}	Soft power-off current	AVDD=DVDD=TVDD=PVDD=5V Opening of RF level detector	—	1.5	—	uA
I_{IDLE}	Idle current	AVDD=DVDD=TVDD=PVDD=5V	—	2.5	—	mA
I_{DVDD}	Digital power current	DVDD=5V	—	2.2	—	mA
I_{AVDD}	Analog power current	AVDD=5V, in case of RCVOff=0	—	2.1	—	mA
	Analog power current	AVDD=5V, in case of RCVOff=1	—	2.07	—	mA
I_{TVDD}	Transmitter power current	Continuous emission of carrier, TVDD=5V	—	230	300	mA
V_{Ripple}	Power ripple resistance				300	mV
V_{Noise}	Anti-power random noise				1600	mV
R_{TX}	TX1/TX2 output resistance			20		Ω
V_{RX}	RX input sensitivity	f_{SUB}=848kHz		0.5		mVrms
R_{Rx}	Rx input resistance			50		K Ω
V_{POR}	Power-on resetting voltage			1.5		V
T_{OSU}	Starting time of crystal oscillator			300		us

Examples of low consumption applications

Card type	Height of card swiping vs. Working current						
	1 cm	2 cm	3 cm	4 cm	5 cm	6 cm	7 cm
S50	10 mA	10 mA	12 mA	15 mA	17 mA	21 mA	25 mA
S70	10 mA	10 mA	12 mA	15 mA	17 mA	21 mA	25 mA
Ultra Light	12 mA	12 mA	14 mA	15 mA	21 mA	25 mA	27 mA

Note:

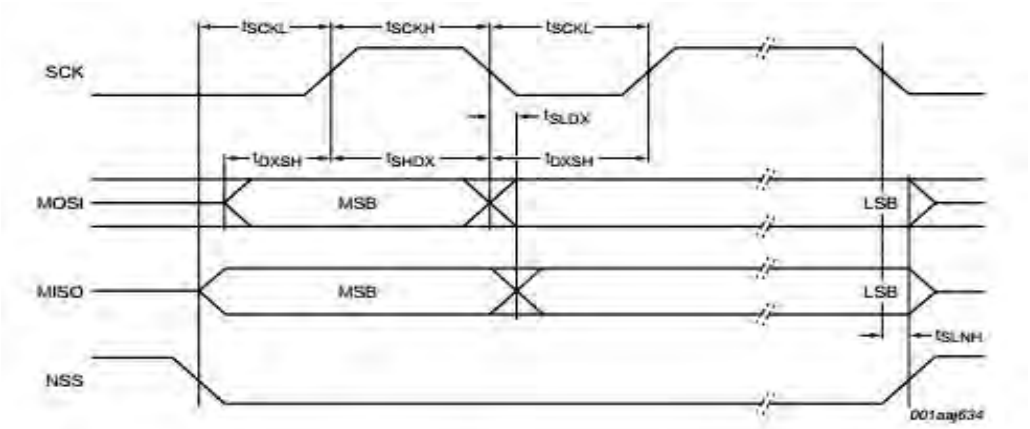
[1] The specific distance of card swiping is influenced by the antenna size and tuning;

[2] Under the same distance, the introduced load is different due to the different inductive reactance's of different cards, further causing different currents of card reader.

SPI timing characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
t_{SCKL}	pulse width LOW	line SCK	50	-	-	ns
t_{SCKH}	pulse width HIGH	line SCK	50	-	-	ns
t_{SHDX}	SCK HIGH to data input hold time	SCK to changing MOSI	25	-	-	ns
t_{DXSH}	data input to SCK HIGH set-up time	changing MOSI to SCK	25	-	-	ns
t_{SLDX}	SCK LOW to data output hold time	SCK to changing MISO	-	-	25	ns
t_{SLNH}	SCK LOW to NSS HIGH time		25	-	-	ns
t_{NHNL}	NSS HIGH time	before communication	50	-	-	ns
t_{DOD}	Data out delay			20		ns
t_{DOHZ}	Data out to high impedance delay			20		ns

SPI timing diagram



Note:

[1] The signal NSS must be LOW to be able to send several bytes in one data stream.

[2] To send more than one data stream NSS must be set HIGH between the data streams.

IO Electrical characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
EA, I2C, EN						
I_{LEAK}	Input leak current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
MFIN						
I_{LEAK}	Input leak current	Operating/sleeping mode pin connects with VDD	-1	-	1	uA
		Operating/sleeping mode pin connects with GND		14.1		uA
		Operating/sleeping mode pin connects with the voltage of 1.5V		13.1		uA

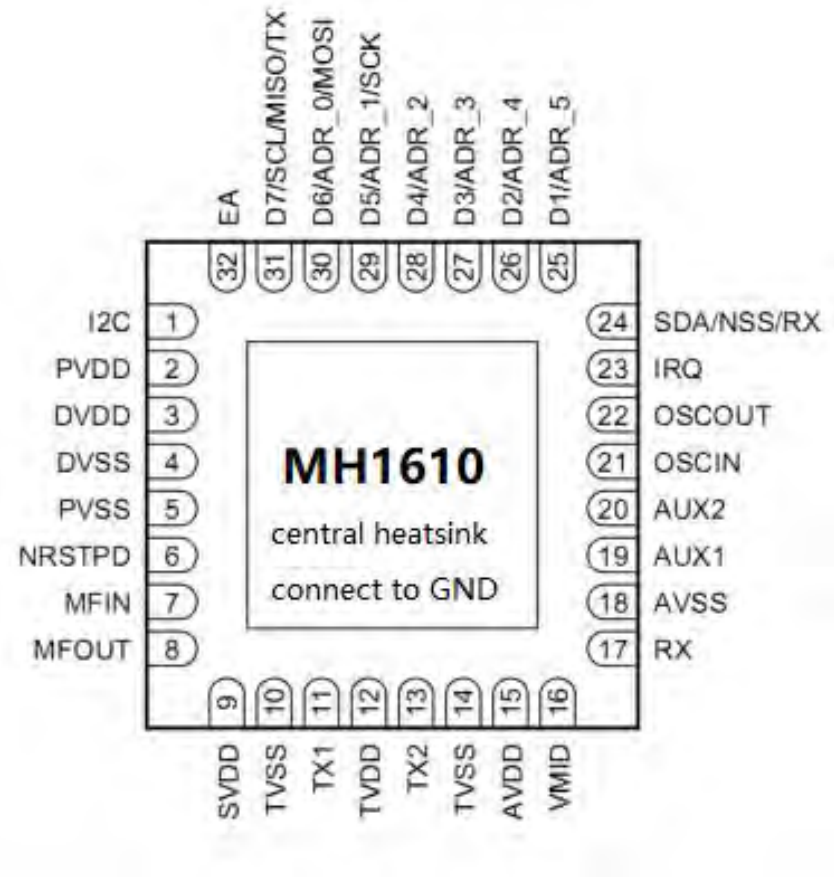
		Operating/sleeping mode pin is hung in the air		0		uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
NSS						
I_{LEAK}	Input leak current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
OSCIN						
I_{LEAK}	Input leak current	Working mode pin connects with VDD		1.1		uA
		Working mode pin connects with GND		0.6		uA
		Operating mode pin connects with the voltage of 1.5V		0.4		uA
		Working mode pin is hung in the air	-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
D1, D2, D3, D4						
I_{LEAK}	Input leak current	Operating/sleeping mode pin connects with VDD	-1	-	1	uA
		Operating/sleeping mode pin connects with GND		13.5		uA
		Operating/sleeping mode pin connects with the voltage of 1.5V		13		uA
		Operating/sleeping mode pin is hung in the air		0		uA
V_{IH}	Input voltage		0.7PVDD			V

	high level					
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V; I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V; I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
I_{OH}	High level output current	VDD(PVDD) = 3 V	-8.5		-7.3	mA
I_{OL}	Low level output current	VDD(PVDD) = 3 V	7.3		8.5	mA
SCK, SDI						
I_{LEAK}	Input leak current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
SDO						
I_{LEAK}	Input leak current	Operating/sleeping mode pin connects with VDD		13.4		mA
		Operating/sleeping mode pin connects with GND	-1	-	1	uA
		Operating/sleeping mode pin connects with the voltage of 1.5V		12.72		mA
		Operating/sleeping mode pin is hung in the air	-1	-	1	uA
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V; I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V; I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
MFOUT, IRQ						
I_{LEAK}	Input leak		-1	-	1	uA

	current					
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V; I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V; I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
I_{OH}	High level output current	VDD(PVDD) = 3 V	-8.5		-7.3	mA
I_{OL}	Low level output current	VDD(PVDD) = 3 V	7.3		8.5	mA
OSCOUT						
I_{LEAK}	Input leak current	Working mode pin connects with VDD		8.01		mA
		Working mode pin connects with GND		2.49		mA
		Operating mode pin connects with the voltage of 1.5V		3.3		mA
		Working mode pin is hung in the air	-1	-	1	uA
I_{LEAK}	Input leak current	Working mode pin connects with VDD		8.35		mA
		Sleeping mode pin connects with GND	-1	-	1	uA
		Sleeping mode pin connects with the voltage of 1.5V		3.7		mA
		Sleeping mode pin is hung in the air	-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high	V_{DD}(PVDD)=3V; I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V

	level					
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V; I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V

Pin configuration of QFN32



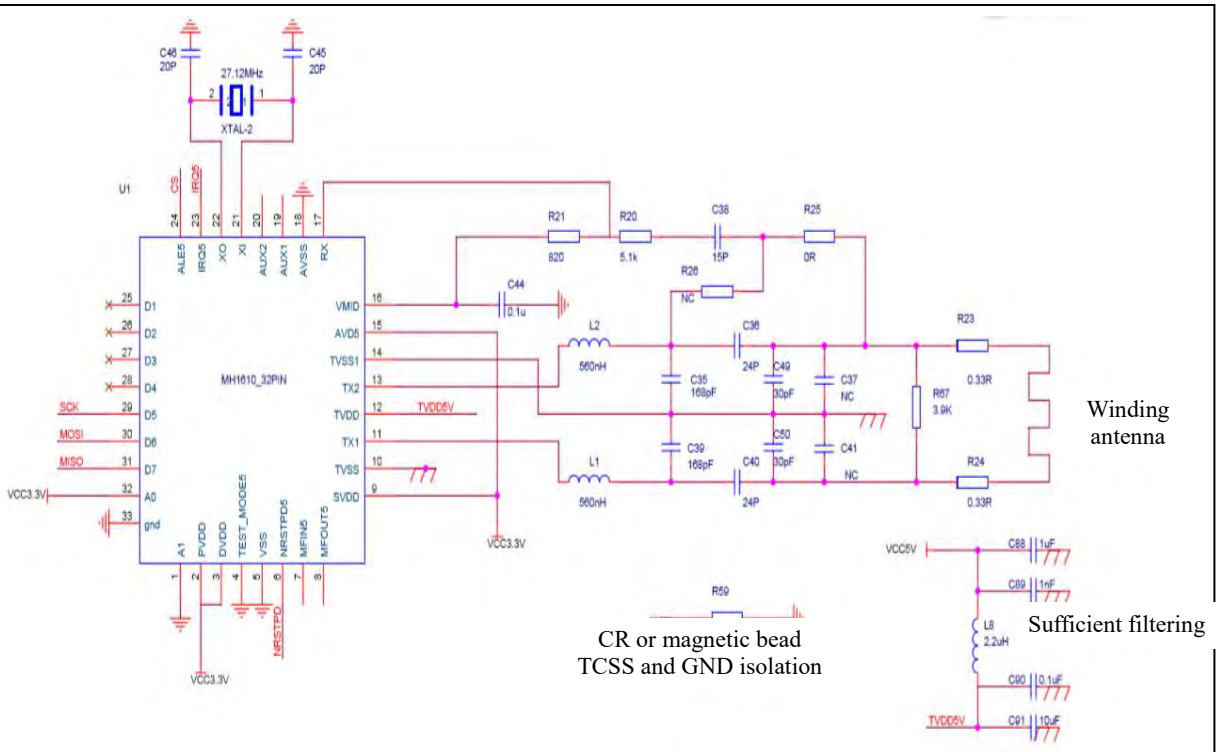
Pin configuration QFN32

Pin description of QFN32

S/N	Symbol	Type	Description
1	I2C	I	I2C Interface enabling
2	PVDD	PWR	Pin power supply
3	DVDD	PWR	Digital power
4	DVSS	PWR	Digital ground
5	PVSS	PWR	Pin power ground
6	NRSTPD	I	Reset or power-down pin, active low
7	MFIN	I	Signal input
8	MFOUT	O	Signal output

9	SVDD	PWR	Power supply of MFIN and MFOUT
10	TVSS	PWR	Ground of transmitter
11	TX1	O	Transmission of modulated energy carrier signal of 13.56MHz
12	TVDD	PWR	Power supply of transmitter
13	TX2	O	Transmission of modulated energy carrier signal of 13.56MHz
14	TVSS	PWR	Ground of transmitter
15	AVDD	PWR	Analog power supply
16	VMID	PWR	Internal reference voltage
17	RX	I	Signal input
18	AVSS	PWR	Analog ground
19	AUX1	O	Test pin
20	AUX2	O	Test pin
21	OSCIN	I	Externally connect with 27.12MHz crystal or clock signal.
22	OSCOUT	O	Externally connect with 27.12MHz crystal
23	IRQ	O	Output interruption signal
24	SDA/NSS/RX	I/O	Communication interface of SPI/I2C/UART/ parallel port
25	D1/ADR_5	I/O	
26	D2/ADR_4	I/O	
27	D3/ADR_3	I/O	
28	D4/ADR_2	I/O	
29	D5/ADR_1/SCK	I/O	
30	D6/ADR_0/MOSI	I/O	
31	D7/SCL/MISO/TX	I/O	
32	EA	I	Encoding I2C address

Application diagram QFN32 of typical SPI communication



Typical periphery

Note:

[1] The read-write distance of MIFARE card that is supported by this type of circuit can reach 9cm, which is influenced by the antenna size and tuning specifically.

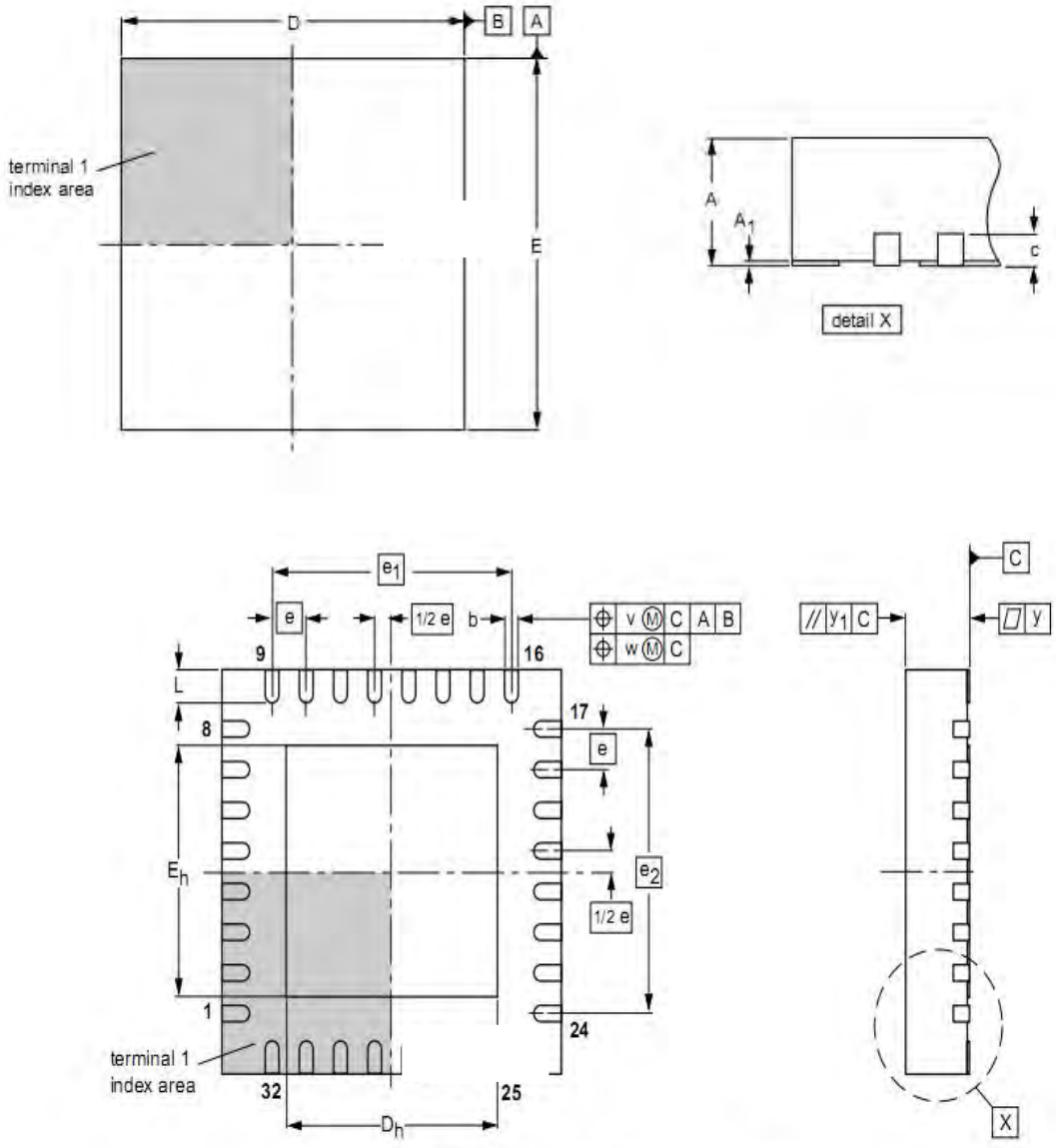
[2] TVSS and GND must be sufficiently isolated.

[3] Power supplies of TVDD, AVDD, SVDD and DVDD need to be sufficiently isolated.

[4] The peripheral matching needs to be re-adjusted as per the different antenna designs.

[5] Under the normal conditions (NC) of resistance R67 of antenna terminal, proper adjustment is available during the passing of EMV3.0 certification.

Package size



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

QFN32 package size