eMMC 5.1

Version 1.0

Apr. 09, 2026

AEM512TDAS-9FMR

128 GB

Revision History

Revision	Date	Description	Editor
1.0	Apr. 09, 2026	Initial release	Danny Sung

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Key Features

- **Capacity:**
  - 128 GB
- **NAND Flash:**
  - 3D NAND TLC
- **Form Factor:**
  - 11.5mm x 13mm x 1.0mm
- **Package:**
  - FBGA 153 ball
- **Interface:**
  - eMMC 5.1
- **Flash Management:**
  - LDPC ECC Engine
  - Bad block Management
  - Garbage collection
  - TRIM Command
  - Wear-leveling
  - IOPS optimization
  - Read sensing
- **Double data rate function:**
  - HS400
- **Data bus widths:**
  - 1 bit, 4 bit, 8 bit
- **Memory Power(VCC):**
  - 3.3V (2.7V~3.6V)
- **Interface Power(VCCQ):**
  - 1.8V (1.7V~1.95V)
  - 3.3V (2.7V~3.6V)
- **Performance:**
  - 128 GB: Read 315MB/s;

    Write 250MB/s Note1,2,3
- **Temperature:**
  - Operating: -25°C ~ 85°C
  - Non-operation: -40°C ~ 85°C

Note 1: Values given from an 8-bit bus width, running HS400 mode from ADATA proprietary tool, V_{CC}=3.3V, V_{CCQ}=1.8V.
Note 2: For performance numbers under other test conditions, please contact ADATA representatives.
Note 3: Performance numbers might be subject to changes without notice.

1.0 General Description

This product is ADATA's most advanced eMMC flash storage solution, combining an embedded flash controller and 3D NAND flash memory, with eMMC 5.1 interface.

Empowered with eMMC 5.1 feature set such as HS400 mode, the product is the optimal device for reliable code and data storage. In addition to high reliability and high system performance offered by the current ADATA eMMC family of products, product support for multiple NAND technology transitions, as well as features such as an advanced power management scheme. Product provides high random access speed, advanced flow control capability, more powerful computing power. The hardware ECC engine implements intelligent flash management and improves the NAND flash endurance. With enhanced vendor command support and embedded test modes, product brings high flexibility for customized usage and failure analysis.

Product is well-suited to meet the needs of small, low power, electronic devices. With JEDEC form factors measuring 11.5mm x 13mm (153 balls) compatible with 0.5mm ball pitch. The product is suitable for a wide variety of electronic devices such as smartphones, tablets, PDAs, eBook readers, digital cameras, recorders, MP3, MP4 players, electronic learning products, digital TVs and set-top boxes.

2.0 Mechanical Specifications

All product specifications not covered in this document (electrical performance, appearance, etc.) are in accordance with ADATA's defined norms and standards.

2.1 Physical Dimensions and Weights

Table 2-1 Dimensions and Weights

Capacity(GB)	Length(mm)	Width(mm)	Height(mm)
128 GB	13±0.1	11.5±0.1	1.0 (Max)

2.2 Product Dimensions

Figure 2-1 Top View

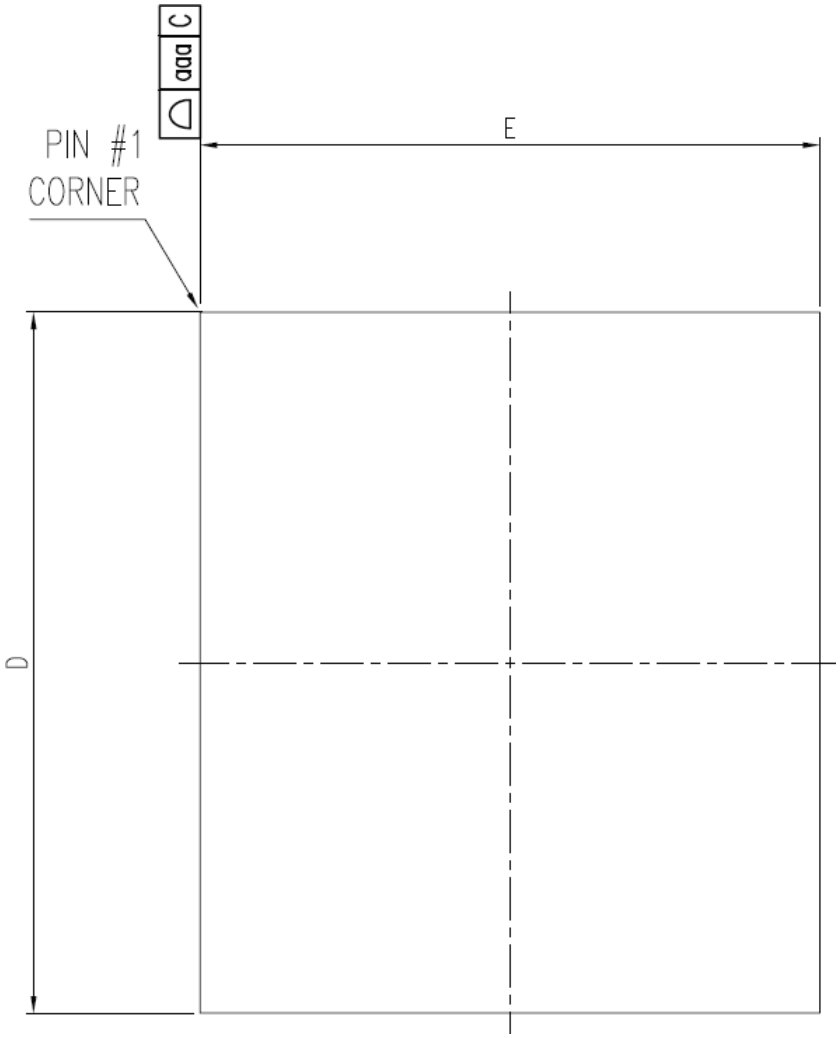


Figure 2-2 Bottom View

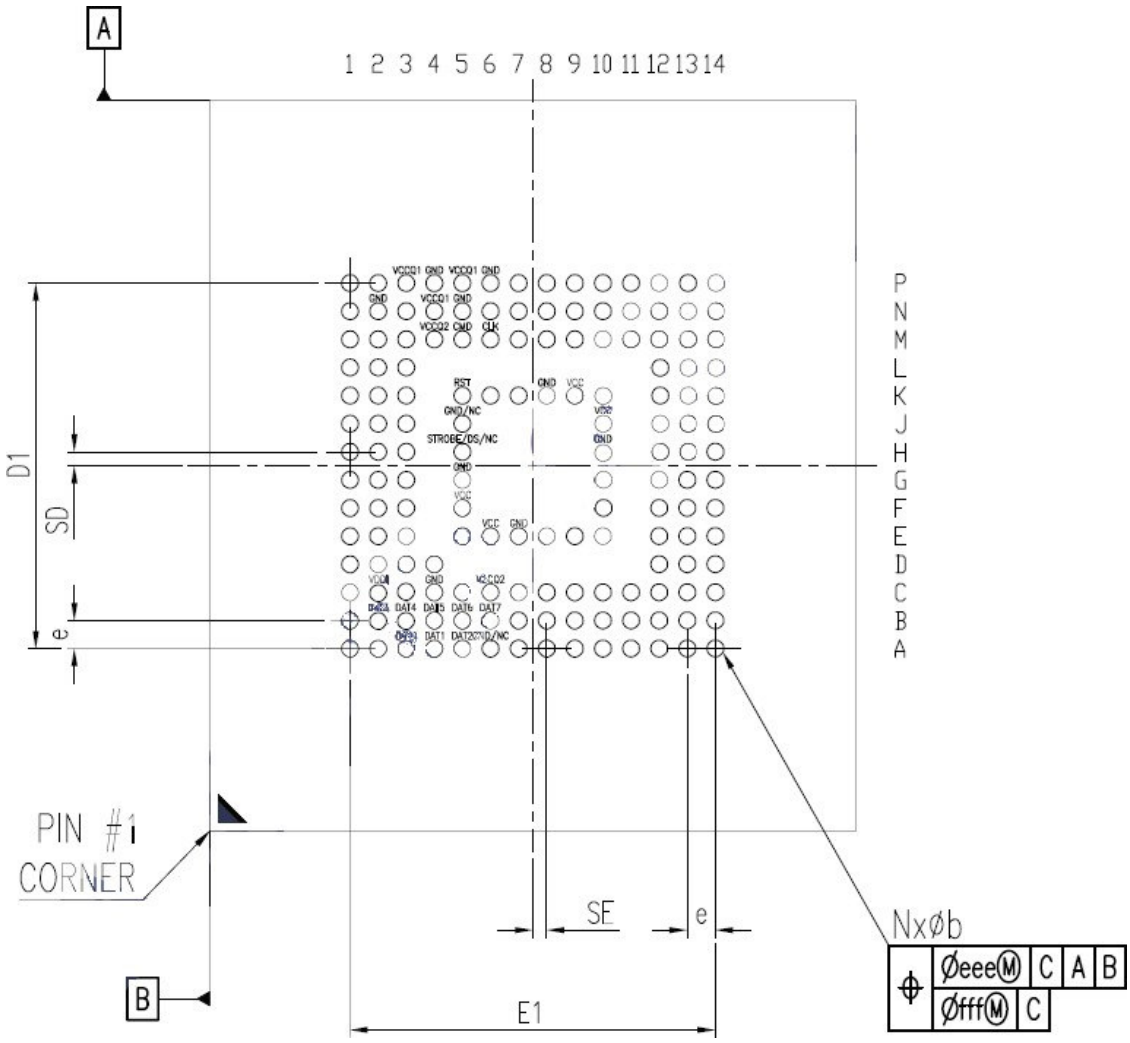


Figure 2-3 Side View

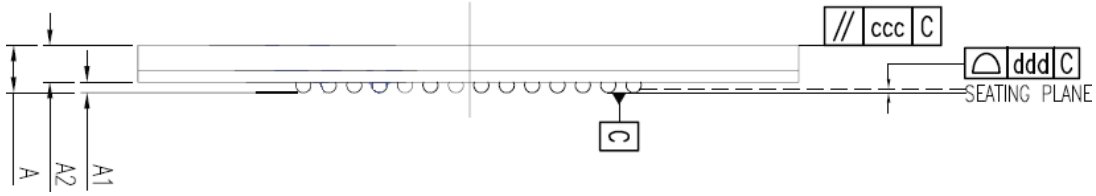


Table 2-2 Form Factor 11.5mm x 13mm x 1.0mm Dimensions

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.85	1.00	0.028	0.033	0.039
A1	0.17	0.22	0.27	0.007	0.009	0.011
A2	0.53	0.63	0.73	0.021	0.025	0.029
b	0.27	0.32	0.37	0.011	0.013	0.015
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.50 BSC.			0.020 BSC.		
JEDEC	MO-276(REF.)/MM					
aaa	0.15					
ccc	0.20					
ddd	0.08					
eee	0.15					
fff	0.05					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
153L	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.

3.0 Product Specifications

3.1 Interface and Configurations

- Compliant with JEDEC eMMC Industry Standard 5.1

3.2 Capacity

Table 3-1 User Addressable Sectors

Model	AEM512TDAS-9FMR
Unformatted Capacity	128 GB
Total User Addressable Sectors (LBA Mode)	244,285,184
User Density	125,074,145,280 Bytes

Total useable capacity may be less (due to formatting, flash management, and other functions). 1GB=1,000,000,000 bytes; 1sector = 512bytes.

3.3 Performance

3.3.1 CDM Performance

Table 3-2 Read/Write Performance (HS400)

	128 GB	Unit
Sequential Read	315	MB/s
Sequential Write	250	MB/s

- Note 1: Values given from an 8-bit bus width, running HS400 mode from ADATA proprietary tool, V_{CC}=3.3V, V_{CCQ}=1.8V.
- Note 2: For performance numbers under other test conditions, please contact ADATA representatives.
- Note 3: Performance numbers might be subject to changes without notice.

3.4 Electrical Specifications

3.4.1 Power Supply Voltage and Power Consumption

The device interface supports the MMC protocol. For more information regarding these buses, refer to JEDEC Standard No. JESD84-B51.

Table 3-4 Power Supply Voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ (Low)	1.7	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.3	0.3	V

Table 3-5 Power Consumption VCC/VCCQ

Parameter	Power	128 GB	Units
Seq. Read Active HS400	ICC	80	mA
	ICCQ	155	mA
Seq. Write Active HS400	ICC	135	mA
	ICCQ	90	mA

Table 3-7 Power Consumption Standby VCC/VCCQ

Supply Voltage	Conditions	128 GB	Units
Standby Current ICC	Sleep	115	uA
Standby Current ICCQ		70	uA

- Note 1: Values given from an 8-bit bus width, a clock frequency of 200MHz DDR mode, V_{CC}=3.3V±5%, V_{CCQ}=1.8V±5%.
- Note 2: Standby current is measured at V_{CC}=3.3V±5%, 8-bit bus width without clock frequency.
- Note 3: Current numbers might be subject to changes without notice.
- Note 4: The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.
- Note 5: This is not 100% test

3.4.2 General DC Characteristics

Table 3-8 General DC Characteristics for eMMC

Parameter	Min	Type	Max	Unit	Remark
Supply voltage for high voltage range	2.7	3.3	3.6	V	
Supply voltage for low voltage range	1.7	1.8	1.95	V	
Supply voltage for core	0.99	1.1	1.21	V	
I/O input leakage current	-10	-	10	µA	
I/O output leakage current	-10	-	10	µA	
Programmable pull-up resistor	28	40	52	kΩ	VCCQ = 3.3V
Programmable pull-down resistor	28	40	52	kΩ	VCCQ = 3.3V
Programmable pull-up resistor	55	80	105	kΩ	VCCQ = 1.8V
Programmable pull-down resistor	55	80	105	kΩ	VCCQ = 1.8V
Pre-initial standby current	-	350	-	µA	
Post-initial standby current	-	100	-	µA	VCCQ > 1.65V
Sleep current	-	100	-	µA	
Operating temperature	-25	+25	+85	°C	
Storage temperature	-40	-	+85	°C	

3.4.3 Bus Signal Levels

Figure 3-1 Bus Signal Levels

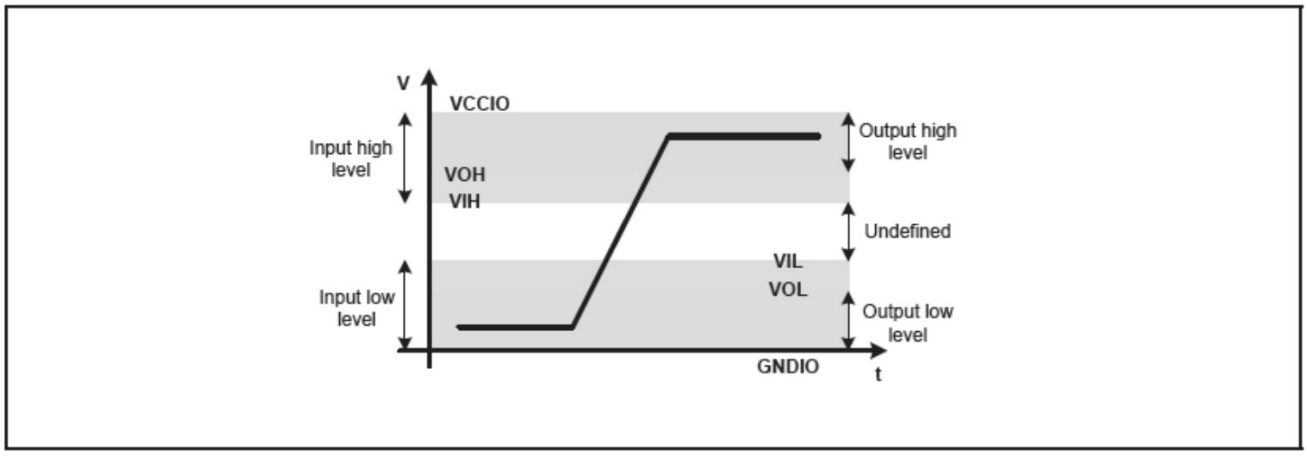


Table 3-9 Bus Signal Levels

Parameter	Symbol	Min	Max	Unit	Remark
Open-drain bus signal level					
Output HIGH voltage	VOH	VCCIO - 0.2	-	V	-
Output LOW voltage	VOL	-	0.3	V	IOL = 2 mA
Push-pull bus signal level (2.7V~3.6V)					
Output HIGH voltage	VOH	0.75 * VCCIO	-	V	IOH = -100 µA at VCCIO min

Output LOW voltage	VOL	-	0.125 * VCCIO	V	IOL = 100 µA at VCCIO min
Input HIGH voltage	VIH	0.625 * VCCIO	VCCIO + 0.3	V	-
Input LOW voltage	VIL	GNDIO - 0.3	0.25 * VCCIO	V	-
Push-pull bus signal level (1.7V~1.95V)					
Output HIGH voltage	VOH	VCCIO - 0.45	-	V	IOH = -2 mA
Output LOW voltage	VOL	-	0.45	V	IOL = 2 mA
Input HIGH voltage	VIH	0.65 * VCCIO	VCCIO + 0.3	V	
Input LOW voltage	VIL	GNDIO - 0.3	0.35 * VCCIO	V	

3.5 Bus Timing

Figure 3-2 Bus Timing in Single Data Rate Mode

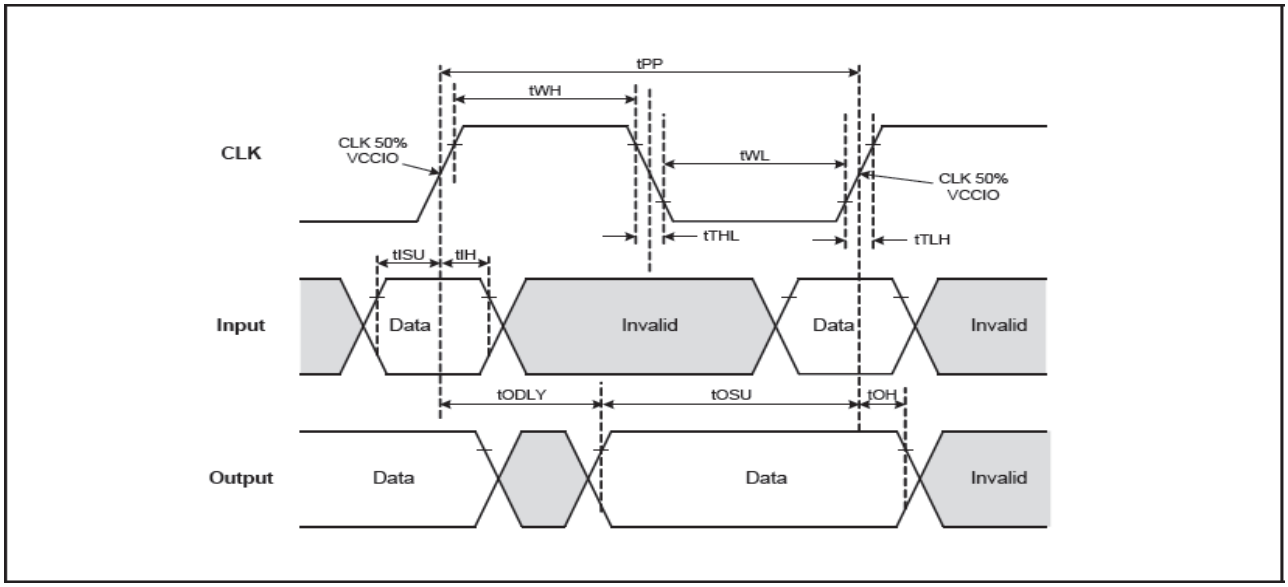


Table 3-10 High Speed Card Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock frequency data transfer mode	f_{PP}	0	52	MHz	C-Load ≦ 30 pF Tolerance +100 KHz
Clock frequency identification mode	f_{OD}	0	400	kHz	Tolerance +20 KHz
Clock high time	t_{WH}	6.5	-	ns	C-Load ≦ 30 pF
Clock low time	t_{WL}	6.5	-	ns	C-Load ≦ 30 pF
Clock rise time	t_{TLH}	-	3	ns	C-Load ≦ 30 pF
Clock fall time	t_{THL}	-	3	ns	C-Load ≦ 30 pF
2.7 ≦ VCCIO ≦ 3.6V					

Input set-up time	t_{ISU}	3	-	ns	C-Load ≦ 30 pF
Input hold time	t_{IH}	3	-	ns	C-Load ≦ 30 pF
Output delay time	t_{ODLY}	-	13.7	ns	C-Load ≦ 30 pF
Output hold time	t_{OH}	2.5	-	ns	C-Load ≦ 30 pF
Signal rise time	t_{RISE}	-	3	ns	C-Load ≦ 30 pF
Signal fall time	t_{FALL}	-	3	ns	C-Load ≦ 30 pF
1.7 ≦ VCCIO ≦ 1.95V					
Input set-up time	t_{ISU}	3	-	ns	C-Load ≦ 30 pF
Input hold time	t_{IH}	3	-	ns	C-Load ≦ 30 pF
Output delay time	t_{ODLY}	-	13.7	ns	C-Load ≦ 30 pF
Output hold time	t_{OH}	2.5	-	ns	C-Load ≦ 30 pF
Signal rise time	t_{RISE}	-	3	ns	C-Load ≦ 30 pF
Signal fall time	t_{FALL}	-	3	ns	C-Load ≦ 30 pF

Table 3-11 Backward Compatible Card Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock frequency data transfer mode	f_{PP}	0	26	MHz	C-Load ≦ 30 pF
Clock frequency identification mode	f_{OD}	0	400	kHz	-
Clock high time	t_{WH}	10	-	ns	C-Load ≦ 30 pF
Clock low time	t_{WL}	10	-	ns	C-Load ≦ 30 pF
Clock rise time	t_{TLH}	-	10	ns	C-Load ≦ 30 pF
Clock fall time	t_{THL}	-	10	ns	C-Load ≦ 30 pF
2.7 ≦ VCCIO ≦ 3.6V					
Input set-up time	t_{ISU}	3	-	ns	C-Load ≦ 30 pF
Input hold time	t_{IH}	3	-	ns	C-Load ≦ 30 pF
Output set-up time	t_{OSU}	11.7	-	ns	C-Load ≦ 30 pF
Output hold time	t_{OH}	8.3	-	ns	C-Load ≦ 30 pF
1.7 ≦ VCCIO ≦ 1.95V					
Input set-up time	t_{ISU}	3	-	ns	C-Load ≦ 30 pF
Input hold time	t_{IH}	3	-	ns	C-Load ≦ 30 pF
Output set-up time	t_{OSU}	11.7	-	ns	C-Load ≦ 30 pF
Output hold time	t_{OH}	8.3	-	ns	C-Load ≦ 30 pF

Figure 3-3 Bus Timing in Dual Data Rate Mode

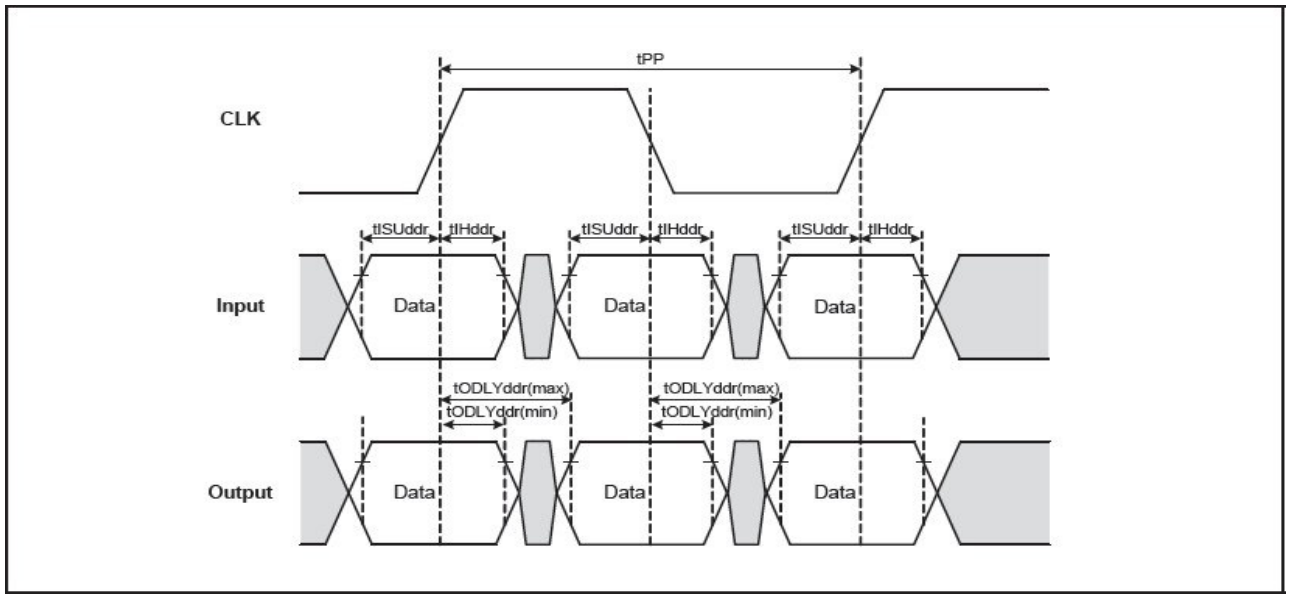


Table 3-12 Dual Data Rate Interface Timing

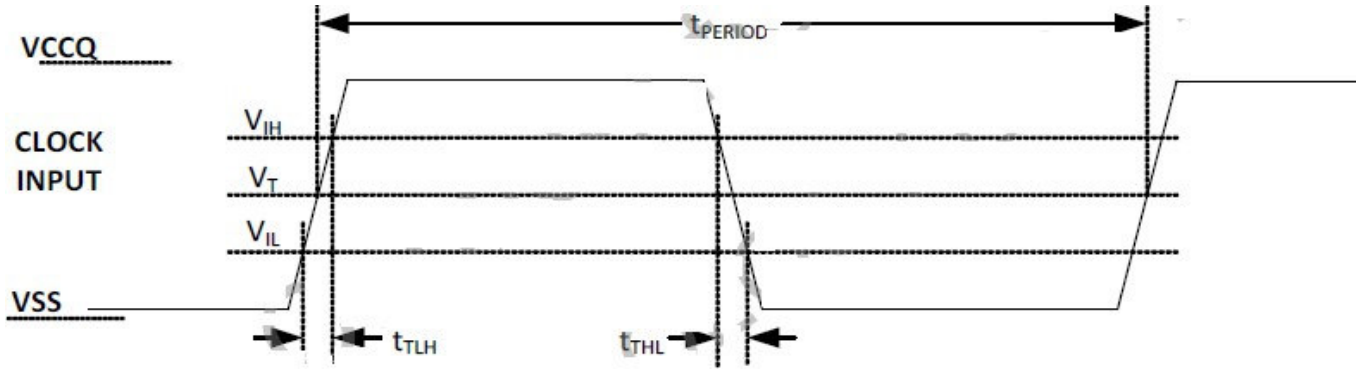
Parameter	Symbol	Min	Max	Unit	Remark
Input CLK[1]					
Clock duty cycle	-	45	55	%	Include jitter, phase noise
Clock rise time	t_{TLH}		3	ns	C-Load ≦ 30 pF
Clock fall time	t_{THL}		3	ns	C-Load ≦ 30 pF
Input CMD (referenced to CLK-SDR mode)					
Input set-up time	tISUddr	3	-	ns	C-Load ≦ 20 pF
Input hold time	tIHddr	3	-	ns	C-Load ≦ 20 pF
Output CMD (referenced to CLK-SDR mode)					
Output delay time during data transfer	tODLY		13.7	ns	C-Load ≦ 20 pF
Output hold time	t_{OH}	2.5		ns	C-Load ≦ 20 pF
Signal rise time	tRISE	-	3	ns	C-Load ≦ 20 pF
Signal fall time	tFALL	-	3	ns	C-Load ≦ 20 pF
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5	-	ns	C-Load ≦ 20 pF
Input hold time	tIHddr	2.5	-	ns	C-Load ≦ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	C-Load ≦ 20 pF
Signal rise time(DAT0-7)[2]	tRISE	-	2	ns	C-Load ≦ 20 pF
Signal fall time(DAT0-7)	tFALL	-	2	ns	C-Load ≦ 20 pF

-Note:

1. CLK timing is measured at 50% of VDD.

2. Inputs DAT rise and fall times are measured by min (V_{IH}) and outputs DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL}).

Figure 3-4 HS200 Clock Signal Timing



-Note:

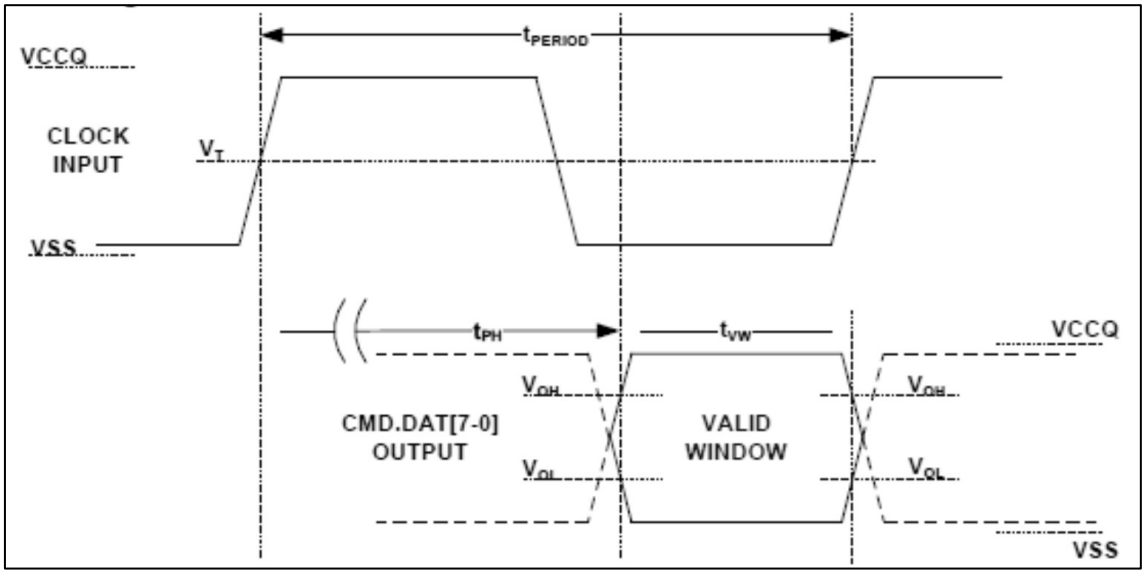
1. VIH denotes VIH(Min.) and VIL denotes VIL(Max).

2. VT=0.975V- Clock Threshold (VCCQ=1.8V),indicates clock reference point for timing measurements.

Table 3-13 HS200 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
tPERIOD	5	-	ns	200MHz(Max.),between rising edges
tTLH,tTHL	-	0.2 · tPERIOD	ns	tTLH,Tthl<1ns(Max.) at 200MHz,CDEVICE=6pF.The absolute maximum value of Ttlh,Tthl is 10ns regard of clock frequency.
Duty cycle	30	70	%	

Figure 3-5 HS200 Device Output Timing



-Note: VOH denotes VOH(min.) and VOL denotes VOL(max.).

Table 3-14 HS200 Device output timing

Symbol	Min	Max	Unit	Remark
tPH	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔTPH	-350 (ΔT= -20 °C)	+1550 (ΔT= 90 °C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (tVW) from last system Tuning procedure ΔTPH is 2600ps for ΔT from -25 °C to 125 °C during operation.
tVW	0.575	-	UI	tVW=2.88ns at 200MHz Using test circuit including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected tVW at Host input is larger than 0.475UI.

-Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz

Figure 3-6 HS400 Device Input Timing

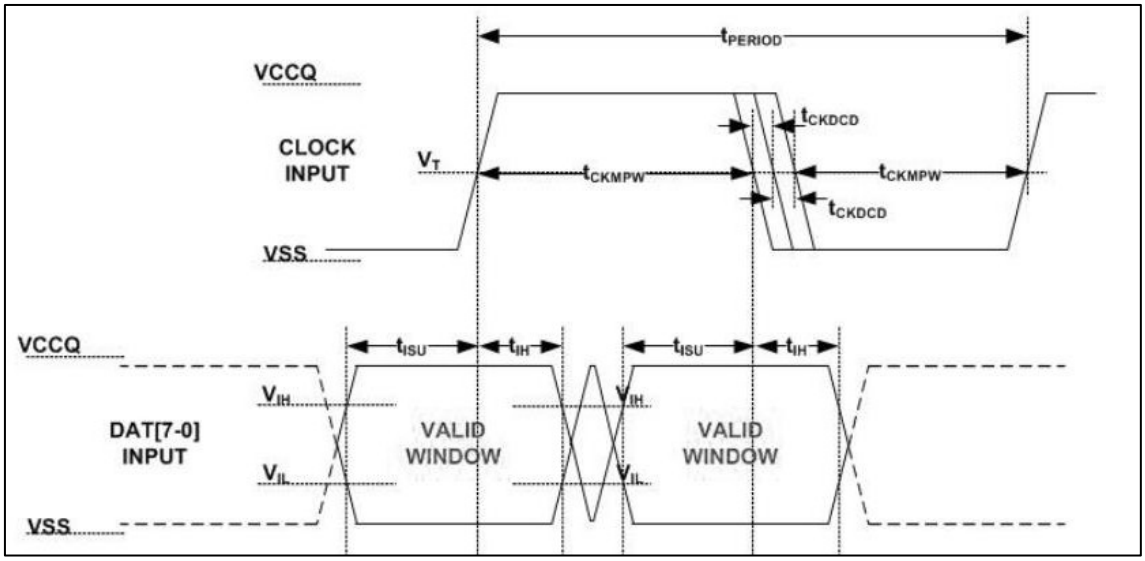


Table 3-15 HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5			200MHz(Max), between rising edges With respect to V_T.
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}
Duty cycle distortion	t_{CKDCD}	0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T. Includes jitter, phase noise
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T.
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4		ns	$C_{Device} \leq 6pF$ With respect to V_{IH}/V_{IL}.
Input hold time	t_{IHddr}	0.4		ns	$C_{Device} \leq 6pF$ With respect to V_{IH}/V_{IL}.
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL}.

Figure 3-7 HS400 Device Output Timing

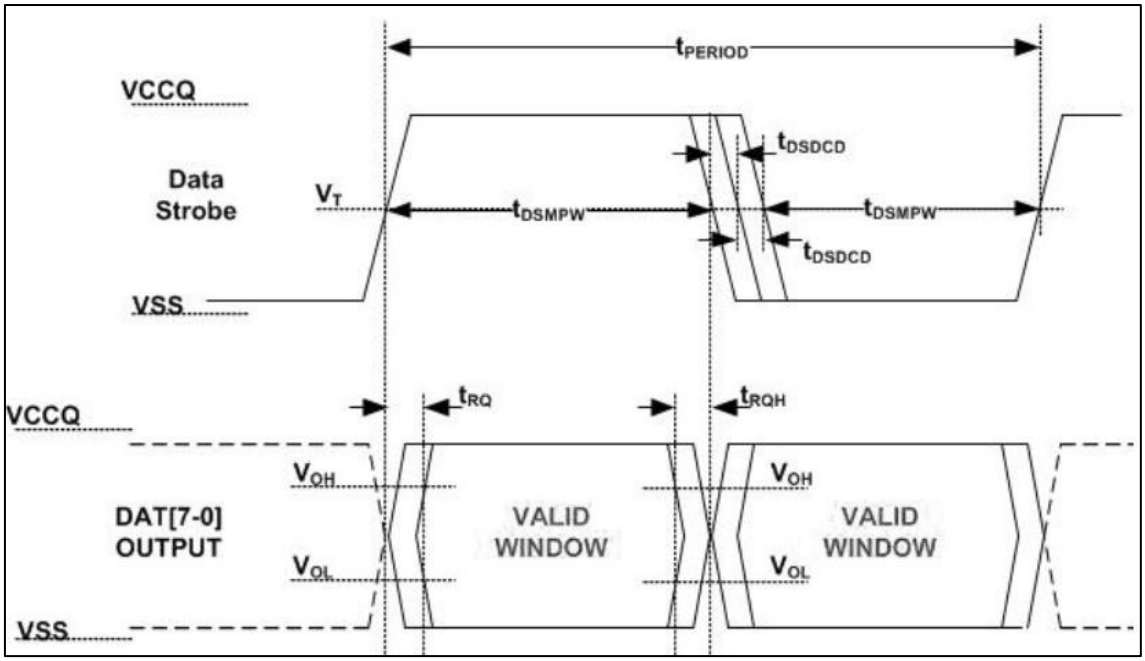


Table 3-16 HS400 Device Output timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5			200MHz(Max), between rising edges With respect to V_T
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (t_{CKDCD}) With respect to V_T Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2.0		ns	With respect to V_T
Read pre-amble	t_{RPRE}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	t_{RPST}	0.4	-	t_{PERIOD}	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Output skew	t_{RQ}	-	0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Output hold skew	t_{RQH}	-	0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load.
Slew rate	SR	1.125	-	V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load

3.6 Power Domains

This product has a dual power input system. VCCQ supplies the eMMC I/O post driver and 1.1V internal core voltage regulator. VCC supplies the NAND Flash I/O post driver and NAND Flash. To achieve a more stable and reliable power system, it is recommended to place a bypass capacitor (At least 0.1µF) for the VCCQ and VCC input. A 1.0µF capacitor for VDDi core power stabilization.

Table 3-17 Power Domains

Pin	Power Domain	Comments
VCCQ	eMMC Interface	Supported voltage ranges: High Voltage Region: 3.3 V (nominal) Low Voltage Region: 1.8 V (nominal)
VCC	Memory	Supported voltage ranges: High Voltage Region: 3.3 V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

4.0 CID Registers

Table 4-1 CID Register Values

Parameter	Bits	Description	Default Value	Width
MID	[127:120]	Manufacturer ID	4Bh	8
CBX	[113:112]	Card BGA	01h	2
OID	[111:104]	OEM/Application	08h	8
PNM	[103:56]	Product Name	128T9F	48
PRV	[55:48]	Product Revision	01h	8
PSN	[47:16]	Product Serial Number	Random by Production	32
MDT	[15:8]	Manufacturing Date	Month, Year	8
CRC	[7:1]	Calculated CRC	Follows JEDEC Standard	7

5.0 Pin assignment and descriptions

5.1 I/F Ball Array

Figure 5-1 eMMC interface in 153 ball array (Top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	NC	DAT0	DAT1	DAT2	VSS	RFU	NC	NC	NC	NC	NC	NC	NC
B	NC	DAT3	DAT4	DAT5	DAT6	DAT7	NC	NC	NC	NC	NC	NC	NC	NC
C	NC	VDDi	NC	VSSQ	NC	VCCQ	NC	NC	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	Index								NC	NC	NC
E	NC	NC	NC		RFU	VCC	VSS	VSF1	VSF2	VSF3		NC	NC	NC
F	NC	NC	NC		VCC					VSF4		NC	NC	NC
G	NC	NC	NC		VSS					VSF5		NC	NC	NC
H	NC	NC	NC		DS					VSS		NC	NC	NC
J	NC	NC	NC		VSS					VCC		NC	NC	NC
K	NC	NC	NC		RESET_n	RFU	RFU	VSS	VCC	VSF6		NC	NC	NC
L	NC	NC	NC									NC	NC	NC
M	NC	NC	NC	VCCQ	CMD	CLK	NC	NC	NC	NC	NC	NC	NC	NC
N	NC	VSSQ	NC	VCCQ	VSSQ	NC	NC	NC	NC	NC	NC	NC	NC	NC
P	NC	NC	VCCQ	VSSQ	VCCQ	VSSQ	NC	NC	NC	VSF7	NC	NC	NC	NC

5.2 Pin Assignments and Pin Type

Table 5-1 Function Pin Assignment, 153 Balls

Ball No.	Ball Signal	Type	Description
A3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
H5	DS	Output	Data Strobe Signal, Used in HS400 mode
K5	RESET_n	Input	Hardware Reset Signal
E6	VCC	Supply	Supply voltage for controller and Flash memory power
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Supply voltage for controller and Flash memory IO power
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
E7	VSS	Supply	Supply voltage ground for controller and Flash memory. Can be short with VSSQ
G5	VSS		
H10	VSS		
K8	VSS		
C4	VSSQ	Supply	Supply voltage ground for controller and Flash memory IO. Can be short with VSS
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
C2	VDDi	Supply	Internal voltage node: At least a 0.1µF capacitor is required to connect VDDi to ground. A 1µF capacitor is recommended. Do not tie to supply voltage or ground

-Note: It's recommended to place a bypass capacitor (At least 0.1µF) for the VCCQ and VCC input. A 1.0µF capacitor is required for VDDi for core power stabilization.

5.3 eMMC Signal and Capacitor Connections and Placement

5.3.1 Decoupling Cap Location recommendation

It is important to place decoupling caps as close to the target power balls as possible. For detailed ball locations, please refer to the Figure 5-2.

5.3.2 Decoupling Cap recommendation

X7R or X5R capacitors are recommended. Rated Voltage : Greater than or equal to 6.3V. Size : As small as possible to close to the BGA power balls.

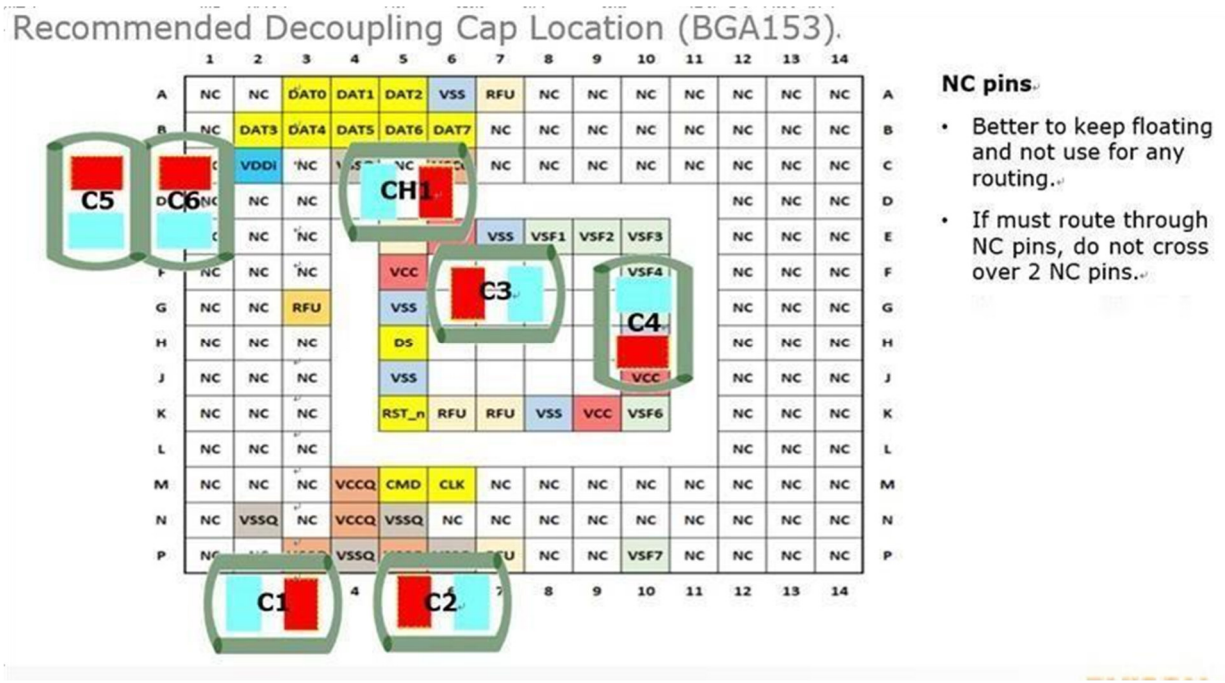
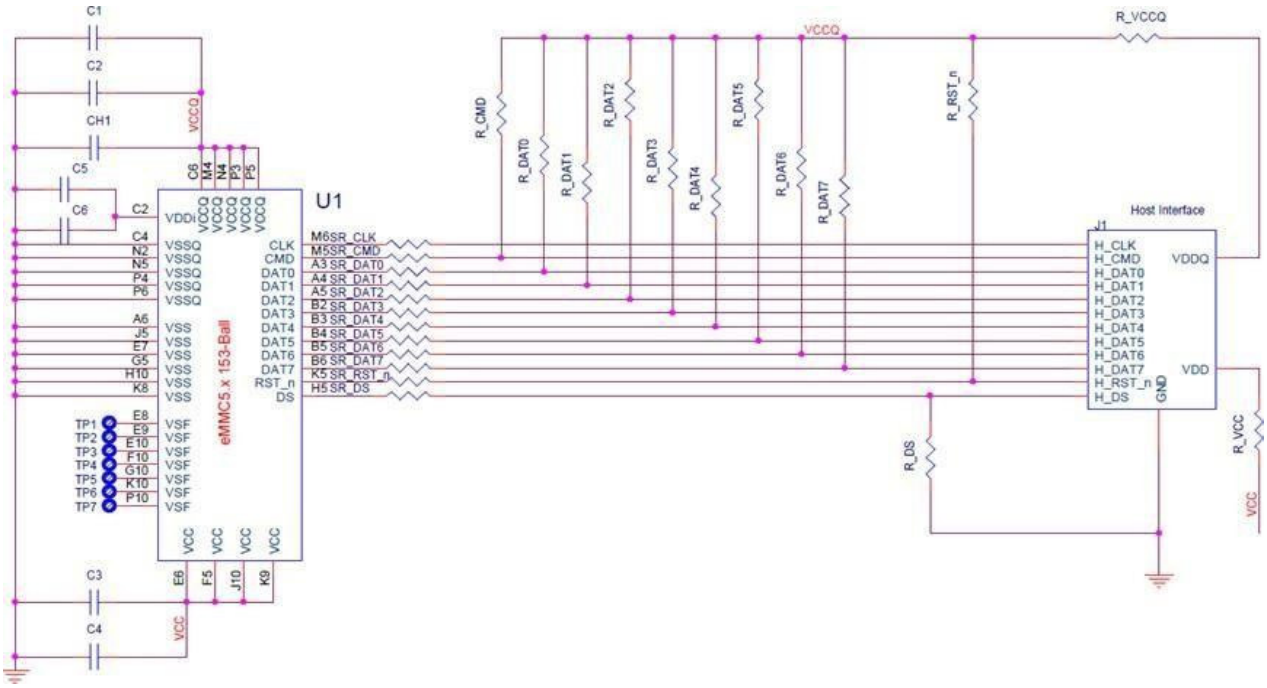


Figure 5-2 Capacitor Location Suggestion (example capacitor size 0402)

5.3.3 Schematic Reference Design

This page is the circuit guide for PCB design, this is only for 153 ball:

E8 to E10、F10、G10、K10 and P10 please keep floating, These pads only for eMMC debug purpose. Do not use it.



Parameter	Symbol	Min	Max	Typ	Units	Remark
Pull-up resistance for CMD	R_CMD	4.7	50	**10**	Kohm	to prevent bus floating
Pull-up resistance for DAT0 - 7	R_DAT	10	50	**10**	Kohm	to prevent bus floating
Pull-up resistance for RST_n	R_RST_n	4.7	50	**10**	Kohm	It is not necessary to put pull-up resistance on RST_n (H/W rest) line if host does not use H/W reset. (Extended CSD register [162] = 0 b)
Pull-down resistance for Data Strobe	R_DS	10	50	**10**	Kohm	
Impedance on CLK / CMD / DAT0~7		45	55	**50**	ohm	Impedance match
Serial's resistance on CLK line	SR_CLK	-	-	**0**	ohm	If customer want to put serial resistance except 0 ohm, they need to check timing are all in SPEC.
Serial's resistance on power trace	R_VCC R_VCCQ	-	-	**0**	ohm	Typeical size 0603 or 0805.
Serial's resistance on CMD / DS / DAT0~7 line / RST_n	SR_RST_n SR_DS SR_CMD SR_DAT0~7	-	-	**0**	ohm	If customer want to put serial resistance except 0 ohm, they need to check timing are all in SPEC.
$V_{CC}Q$ capacitor value	C1	2.2	4. 7	**4.7**	μ F	Coupling capacitor should be connected with
	C2	0.1	0.22	**0.1**	μ F	VDDQ and VSSQ as closely as possible
	CH1	1	2.2	1	μ F	CH1 should be placed adjacent to VccQ-VssQ balls (#C6 and #C4 accordingly, next to DAT[7..0] balls), It should be located as close as possible to the balls defined in order to minimize connection parasitics.
V_{CC} capacitor value	C3	2.2	4. 7	**4.7**	μ F	Coupling capacitor should be connected with
	C4	0.1	0.22	**0.22**	μ F	VDD and VSS as closely as possible
VDDi capacitor value (C_{R93})	C5	1	4.7	**2.2**	μ F	Coupling capacitor should be connected with
	C6	0.1	0.22	**0.1**	μ F	VDDi and VSSi as closely as possible
Vendor Specific	TP1~7	-	-	-	-	The function of these signals is defined and specified by the controller vendor. A pin that is not to be used in normal applications and that may or may not have an internal connection. The VSF signals shall be treated as NU signals by the user. The VSF signals shall reserved test points on the PCB, avcid reference high speed layer and power plane.

Figure 5-3 Recommended schematic design and caps/resistance selection

Note: It doesn't matter to put Pull-up resistance and Serial's resistance closer to host or eMMC. However, it's recommended to put all resistors on the same PCB side (Top or Bottom)

6.0 Ordering Information

Table 6-1 Ordering Information

Model Name	Capacity	Type	Remark
AEM512TDAS-9FMR	128 GB	eMMC FBGA-153	-25°C ~ 85°C

7.0 Package Specifications

Figure 7-1 Package Specification

Put the eMMC into tray, 152pcs per tray, and 10 trays per box. Total 1,520pcs per box.

6 boxes per carton. Total 9,120pcs per carton