MEGAHUNT

MH663
Brief Introduction

Contactless Reader IC

Version: 1.1
Date: 2022-03-02

Megahunt Tehnologies Inc.

History of Revision

Date	Version	Description	Author
2022-02-28	1.00	Completed the first draft	MEGAHUNT

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Overview

MH663 is a highly integrated and ultra-low power contactless reader/writer chip, which works at 13.56MHz and supports contactless reader/writer mode conforming to ISO/IEC 14443 TypeA/B, Felica, ISO/IEC 15693 protocols.

Main functions and characteristics

- Digital working voltage range is 1.8V ~ 5V, analog working voltage range is 1.8V ~ 5V
- Support EMV3.0 certification, including electrical, protocol, and mobile phone compatibility certification tests
- The chip power consumption is extremely low, and the effective communication distance can reach 10cm
- Support ISO/IEC 14443 TypeA protocol
- Support Apple Pay, Samsung Pay and other mobile payment applications
- Support ISO/IEC 14443 TypeB protocol
- Support P2P passive initiator mode of ISO/IEC 18092
- Support Felica card 212K and 424K protocols
- Support ISO/IEC 15693 protocol
- Support ISO 14443 A high transmission rate communication: 106kbit/s, 212kbit/s, 424kbit/s, 848kbit/s
- Support SIGIN/SIGOUT
- Supported host interfaces:
  - 10Mbit/s SPI interface
  - I2C interface, 100kbit/s rate in standard mode
  - Serial UART, transfer rate up to 1228.8kbit/s
- 64-byte transmit and receive FIFO buffers
- Flexible interrupt mode
- Programmable timer
- With three power-saving modes: hardware power-down, software power-down and transmitter power-down
- Built-in temperature sensor to automatically stop RF transmission when the chip temperature is too high
- Use multiple sets of power supplies independent of each other to avoid mutual interference between modules and improve the stability of work
- With CRC and parity check function, built-in CRC co-processor, in line with ISO/1EC14443 and CCITT protocol

- Internal oscillator, connected to 27.12 MHz crystal
- Own programmable I/O pins
- Support Low Power Card Detection (LPCD) function

Working conditions

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Voltage	VSS=TVSS=AVSS=GND=0V PVDD<=VDD<=TVDD	1.8	3.3	6	V
PVDD	Pad voltage		1.8	3.3	6	V
TVDD	Transmitter supply voltage		1.8	3.3	6	V
TA	Operating temperature		-40		+85	℃

[1] PVDD must be less than or equal to VDD and TVDD

[2] Recommended power supply conditions: PVDD=VDD<=TVDD

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
AVDD	Analog Power Buffer	CL load capacitance AVDD ＞100nF		1.8		V
TA	Operating temperature		-40		+85	℃

Electrical Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
3.3V typical						
I_{HPD}	Hard brownout current	PVDD=VDD=TVDD=3.3V NRSTPD=LOW	—	0.02	—	uA
I_{SPD}	Soft power-down current	PVDD=VDD=TVDD=3.3V RF Level detector on	—	2.8	—	uA
I_{IDLE}	Idle current	PVDD=VDD=TVDD=3.3V	—	3	—	mA

I_{TVDD}	Transmitter supply current	Continuous transmit carrier, TVDD=3.3V	—	100	170	mA
V_{Ripple}	Anti power ripple				400	mV
V_{Noise}	Immunity to power supply random noise				1600	mV
R_{TX}	TX1/TX2 output resistance			5		Ω
V_{RX}	RX input sensitivity	f_{SUB}=848kHz		0.5		mVrms
R_{Rx}	Rx input resistance			50		KΩ
V_{POR}	Power-on reset voltage			1.5		V
T_{OSU}	Crystal start-up time			300		us
5V typical						
I_{HPD}	Hard brownout current	AVDD=DVDD=TVDD=PVDD=5V NRSTPD=LOW	—	0.02	—	uA
I_{SPD}	Soft power-down current	AVDD=DVDD=TVDD=PVDD=5V RF Level detector on	—	2.8	—	uA
I_{IDLE}	Idle current	AVDD=DVDD=TVDD=PVDD=5V	—	3	—	mA
I_{TVDD}	Transmitter supply current	Continuous transmit carrier, TVDD=5V	—	230	300	mA
V_{Ripple}	Anti power ripple				300	mV
V_{Noise}	Immunity to power supply random noise				1600	mV
R_{TX}	TX1/TX2 output resistance			5		Ω
V_{RX}	RX input sensitivity	f_{SUB}=848kHz		0.5		mVrms
R_{Rx}	Rx input resistance			50		KΩ
V_{POR}	Power-on reset voltage			1.5		V
T_{OSU}	Crystal start-up time			300		us

Examples of low-power applications

Card type	Swipe height **vs.** Working current						
	1 cm	2 cm	3 cm	4 cm	5 cm	6 cm	7 cm
S50	10 mA	10 mA	12 mA	15 mA	17 mA	21 mA	25 mA

S70	10 mA	10 mA	12 mA	15 mA	17 mA	21 mA	25 mA
Ultra Light	12 mA	12 mA	14 mA	15 mA	21 mA	25 mA	27 mA

Note:

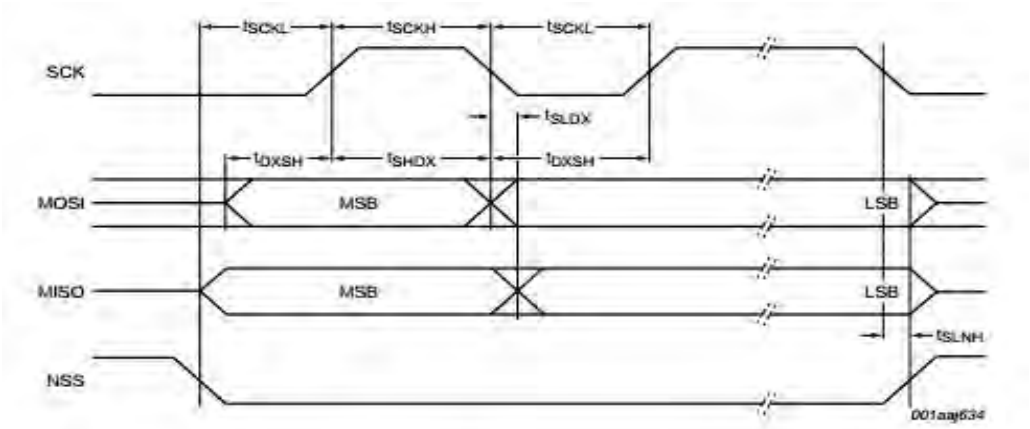
[1] The specific distance of the swipe is affected by the antenna size and tuning;

[2] At the same distance, different cards will introduce different loads due to their different inductive reactances, and thus the current of the card reader will be different.

SPI Timing Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{SCKL}	pulse width LOW	line SCK	50	-	-	ns
t_{SCKH}	pulse width HIGH	line SCK	50	-	-	ns
t_{SHDX}	SCK HIGH to data input hold time	SCK to changing MOSI	25	-	-	ns
t_{DXSH}	data input to SCK HIGH set-up time	changing MOSI to SCK	25	-	-	ns
t_{SLDX}	SCK LOW to data output hold time	SCK to changing MISO	-	-	25	ns
t_{SLNH}	SCK LOW to NSS HIGH time		25	-	-	ns
t_{NHNL}	NSS HIGH time	before communication	50	-	-	ns
t_{DOD}	Data out delay			20		ns
t_{DOHZ}	Data out to high impedance delay			20		ns

SPI Timing diagram



Note:

[1] The signal NSS must be LOW to be able to send several bytes in one data stream.

[2] To send more than one data stream NSS must be set HIGH between the data streams.

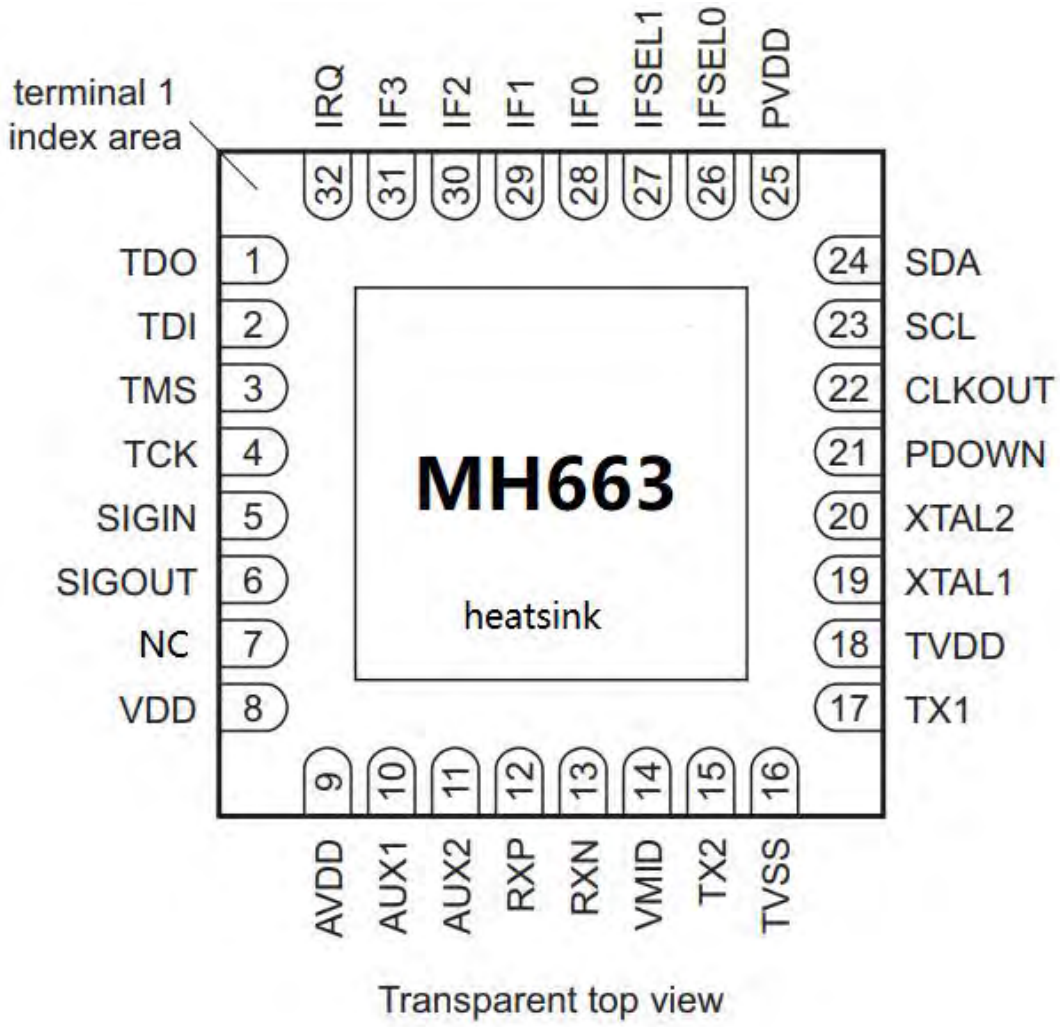
IO Electrical Characteristics

Name	Parameter	Condition	Min.	Typ.	Max.	Unit
IFSEL0，IFSEL1，PDOWN						
I_{LEAK}	Input leakage current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
SIGIN						
I_{LEAK}	Input leakage current	Work/sleep state pin connection VDD	-1	-	1	uA
		Work/sleep state pin connection GND		14.1		uA
		Work/sleep state pin connection 1.5V		13.1		uA
		Work/sleep state pin floating		0		uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
IF3/NSS						
I_{LEAK}	Input leakage current		-1	-	1	uA

V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
XTAL1						
I_{LEAK}	Input leakage current	Working status pin connection VDD		1.1		uA
		Working status pin connection GND		0.6		uA
		Working status pin connection 1.5V		0.4		uA
		Working status pin floating	-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
TDO/OUT0，TDI/OUT1，TMS/OUT2，TCK/OUT3						
I_{LEAK}	Input leakage current	Working status pin connection VDD	-1	-	1	uA
		Working status pin connection GND		13.5		uA
		Working status pin connection 1.5V		13		uA
		Working status pin floating		0		uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V;I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V;I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
I_{OH}	High level output current	VDD(PVDD) = 3 V	-8.5		-7.3	mA
I_{OL}	Low level output current	VDD(PVDD) = 3 V	7.3		8.5	mA
IF1、IF0						
I_{LEAK}	Input leakage current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
IF2						
I_{LEAK}	Input leakage current	Work/sleep state pin connection VDD		13.4		mA
		Work/sleep state pin connection GND	-1	-	1	uA
		Work/sleep state pin connection 1.5V		12.72		mA
		Work/sleep state pin floating	-1	-	1	uA

V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V;I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V;I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
SIGOUT、IRQ						
I_{LEAK}	Input leakage current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V;I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V;I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
I_{OH}	High level output current	VDD(PVDD) = 3 V	-8.5		-7.3	mA
I_{OL}	Low level output current	VDD(PVDD) = 3 V	7.3		8.5	mA
XTAL2						
I_{LEAK}	Input leakage current	Working status pin connection VDD		8.01		mA
		Working status pin connection GND		2.49		mA
		Working status pin connection 1.5V		3.3		mA
		Working status pin floating	-1	-	1	uA
I_{LEAK}	Input leakage current	Working status pin connection VDD		8.35		mA
		Working status pin connection GND	-1	-	1	uA
		Working status pin connection 1.5V		3.7		mA
		Working status pin floating	-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V;I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3V;I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V

Pin arrangement HVQFN32



Pin arrangement **HVQFN32**

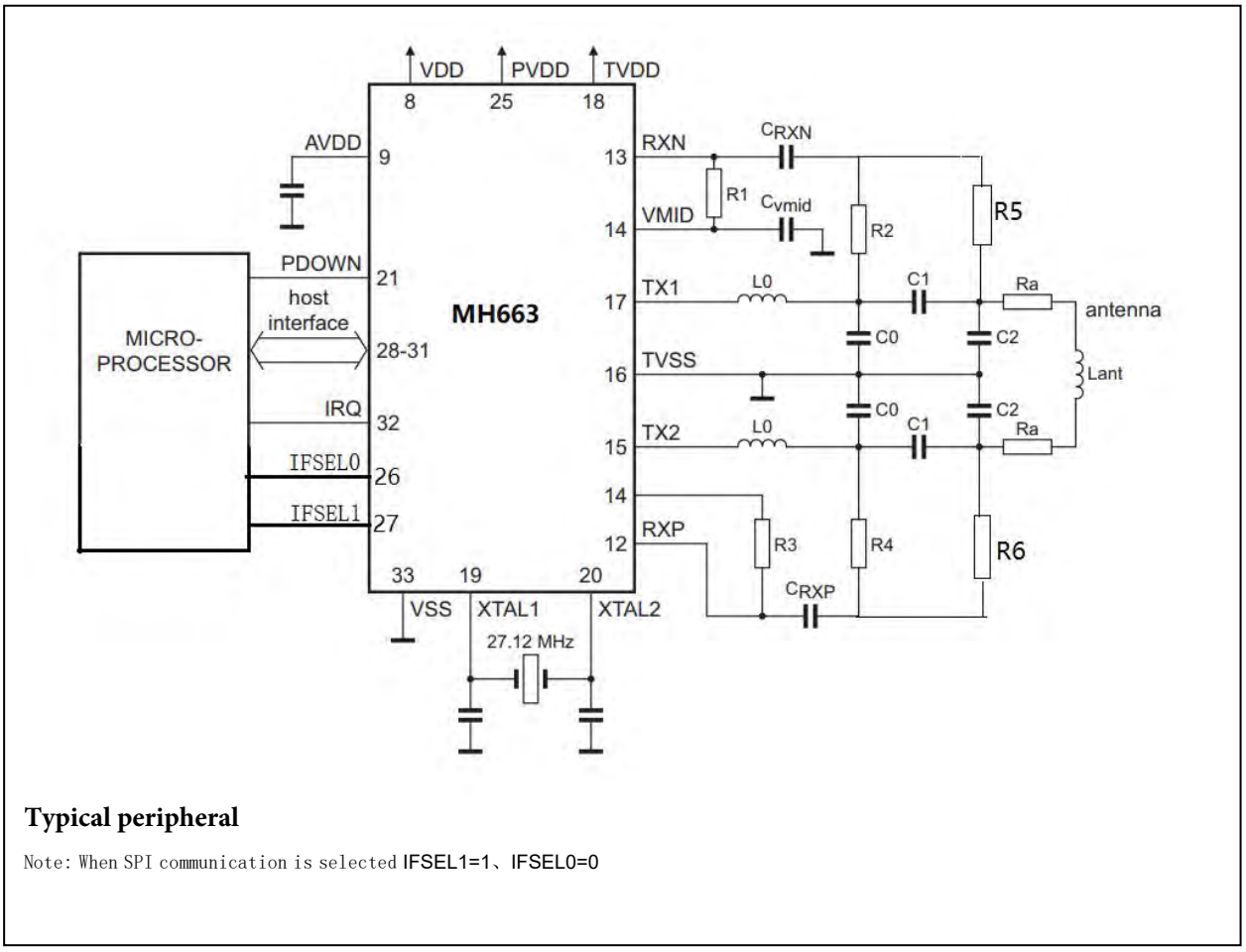
Pin description HVQFN32

Num.	Name	Type	Describe
1	TDO	O	Test Data Output for Boundary Scan Interface
2	TDI	I	Test Data Input for Boundary Scan Interface
3	TMS	I	Test mode selection boundary scan interface

4	TCK	I	Test Clock Boundary Scan Interface
5	SIGIN	I	Contactless communication interface input
6	SIGOUT	O	Non-contact communication interface output
7	NC	NC	Can be suspended
8	VDD	PWR	Power supply
9	AVDD	PWR	Analog Power Buffer
10	AUX1	O	Auxiliary output: pin for analog test signal
11	AUX2	O	Auxiliary output: pin for analog test signal
12	RXP	I	Receiver input pins for receiving RF signals
13	RXN	I	Receiver input pins for receiving RF signals
14	VMID	PWR	Internal receiver reference voltage
15	TX2	O	Transmitter 2:Provides modulated 13.56 MHz carrier
16	TVSS	PWR	Transmitter ground, powers the output stage of TX1, TX2
17	TX1	O	Transmitter 1: Provides modulated 13.56 MHz carrier
18	TVDD	PWR	Transmitter voltage supply
19	XTAL1	I	External 27.12MHz crystal, can be connected to external CL
20	XTAL2	O	External 27.12MHz crystal, can be connected to external CL
21	PDOWN	I	Power-down reset, high-level power-down reset
22	CLKOUT	O	Clock output
23	SCL	O	Serial clock line
24	SDA	I/O	Serial data line
25	PVDD	PWR	Pad power supply
26	IFSEL0	I	Host interface selection
27	IFSEL1	I	Host interface selection
28	IF0	I/O	Interface pins, multi-function pins: can be assigned to the host interface RS232, SPI, I2C, I2C-L
29	IF1	I/O	Interface pins, multi-function pins: can be assigned to host interface SPI, I2C, I2C-L
30	IF2	I/O	Interface pins, multi-function pins: can be assigned to the host interface RS232, SPI, I2C, I2C-L
31	IF3	I/O	Interface pins, multi-function pins: can be assigned to the host interface RS232, SPI, I2C, I2C-L

32	IRQ	O	Interrupt request: output signal interrupt event

Typical SPI communication application diagram HVQFN32

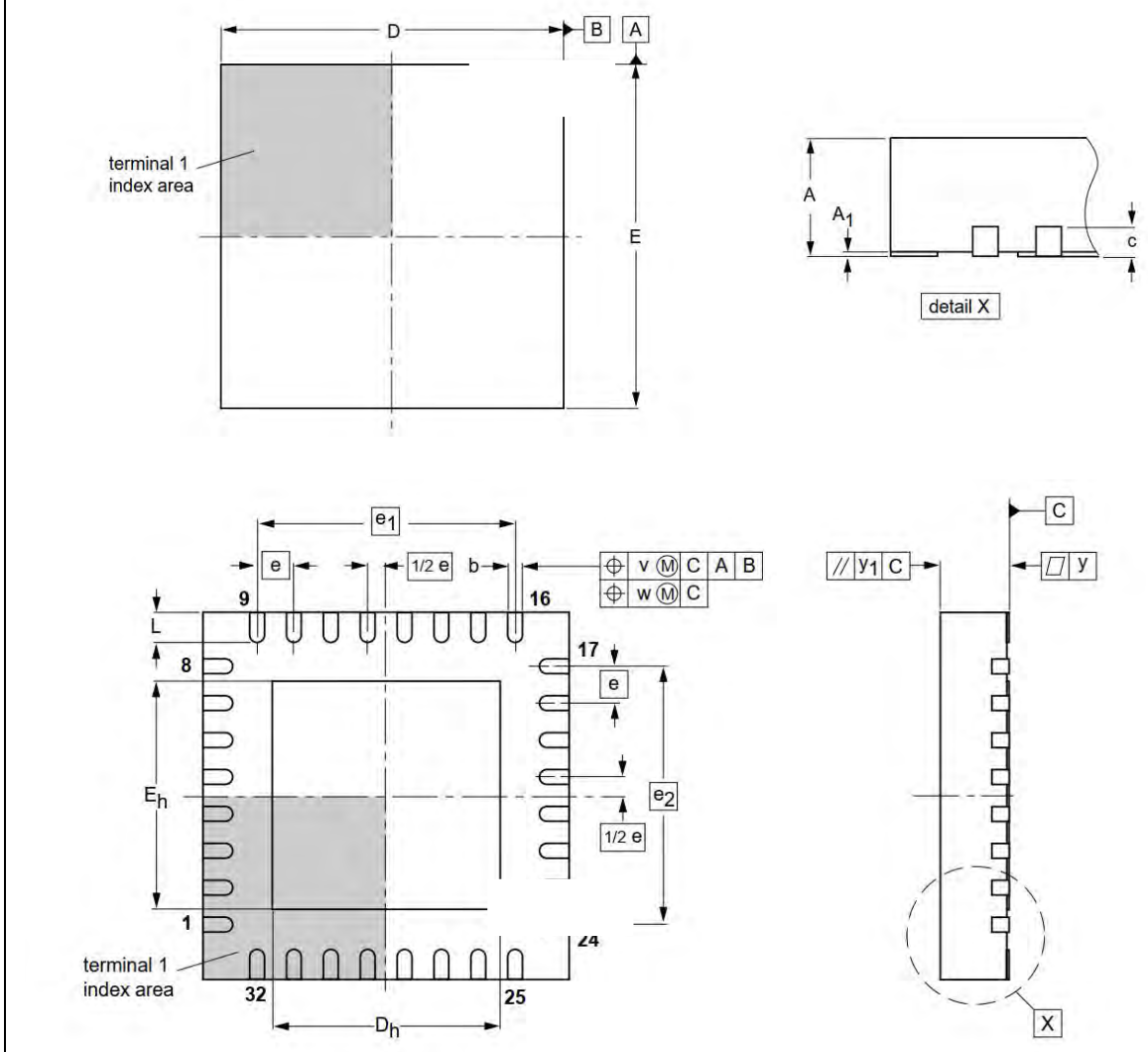


Typical peripheral

Note: When SPI communication is selected IFSEL1=1、IFSEL0=0

Package size HVQFN32

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads;
32 terminals; body 5 x 5 x 0.85 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	e2	L	v	w	y	y1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	---	MO-220	---			~~01-08-08~~ 02-10-18

HVQFN32 Package size