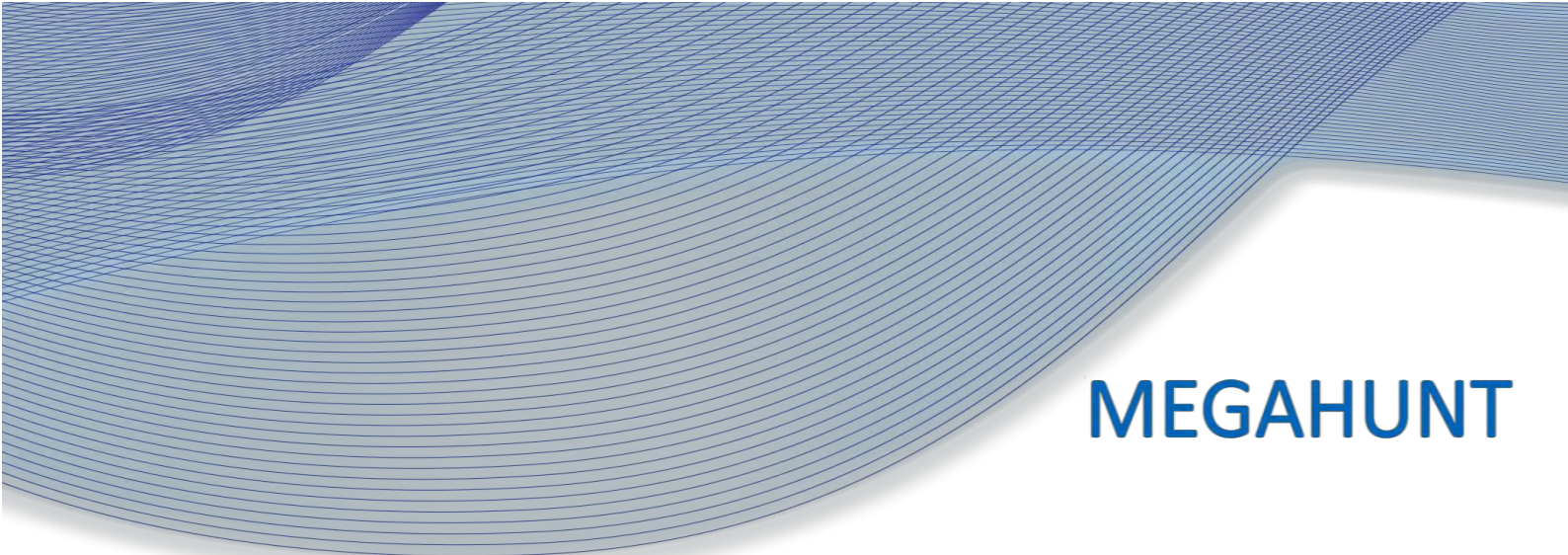


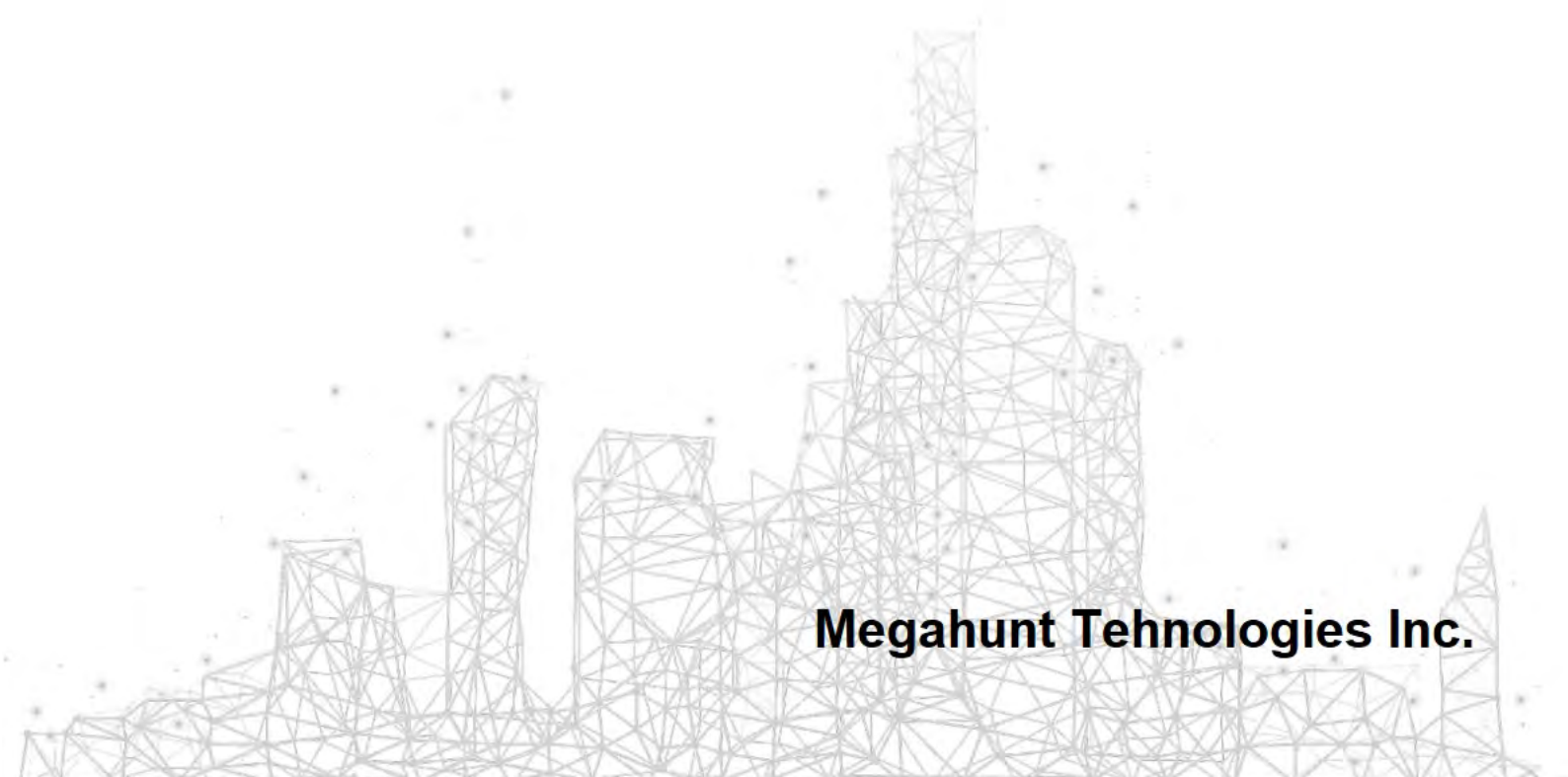


MEGAHUNT

MH1235H

Datasheet

Secure microcontroller with integrated contact smart card reader



Megahunt Tehnologies Inc.

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1. Summary of the Chip

1.1 Chip Description

MH1235H chip is a high security interface chip integrated with contact smart card reader. It provides high security for the card by performing current limit short circuit detection, ESD protection and power monitoring. The chip supports the low power consumption mode, and the current consumption in the low power consumption mode is very low. Therefore, MH1235H is an efficient and ideal contact card reading chip.

1.2 Main Functional Characteristics of the Chip

1.2.1 Protection Contact Smart Card

- Each contact has an overcurrent protection function. When the power pin current is too high, the chip automatically powers down.
- Card end pins support static protection (greater than 8KV)

1.2.2 Simple and Convenient Design

- Support 5V, 3V, 1.8V card voltage
- Chip power supply VDDP wide voltage input 2.7V ~ 5.5V
- Very low power consumption at low power mode < 4 uA
- Support external crystal or MCU input clock, and support fxtal, fxtal/2, fxtal/4, fxtal/8 through frequency division
- Pin OFFN can feedback chip status in time
- CS pin can support multiple MH1235H chips

1.2.3 Others

- QFN32 package form
- Compliant with ISO7816 and EMV4.3 standards

1.3 Chip Applications

- Bank IC card interface chip
- Electronic payment

1.4 Basic Structure of the Chip

The chip system block diagram is as follows:

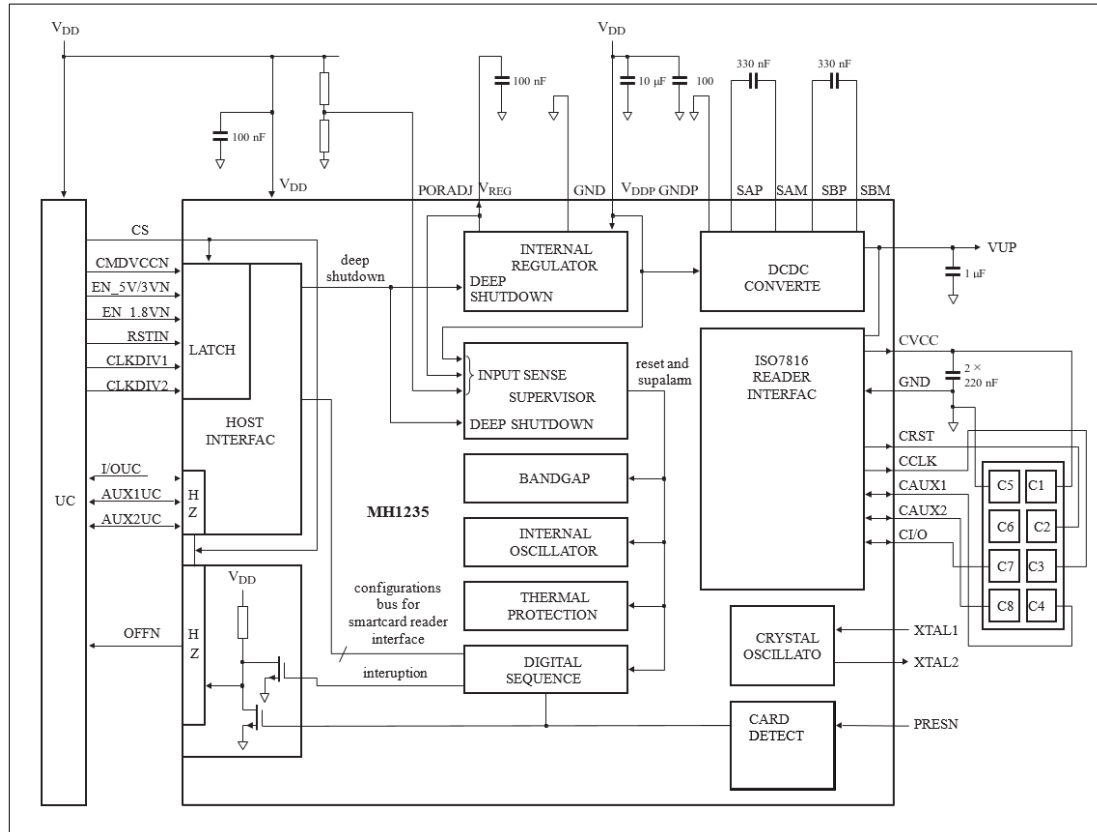


Figure 1. Characteristic Explain

1.5 Chip Parameters

Table 1. Main Parameter Table

$V_{DDP} = 3.3V$; $V_{DD} = 3.3V$; $f_{XTAL} = 4MHz$; $GND = 0V$; $T_{amb} = 25^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
VDDP	Supply voltage		2.7	3.3	5.5	V
VDD	Interface supply voltage		1.6	3.3	3.6	V
VDDP	Supply current	shutdown mode; $f_{XTAL} = \text{stopped}$;	-		180	uA
		active mode; CVCC = +5 V CLK = f_{XTAL} ; no load	-	-	5	mA
		active mode; CLK = f_{XTAL} ; CVCC = +5 V; $I_{CC} = 65\text{ mA}$	-	-	140	mA
		active mode; CLK = f_{XTAL} ; CVCC = +3 V; $I_{CC} = 65\text{ mA}$	-	-	140	mA
		active mode; CLK = f_{XTAL} ; CVCC = +1.8 V; $I_{CC} = 35\text{ mA}$	-	-	80	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DD}	Interface supply current	shutdownmode; f _{XTAL} =stopped; presentcard	-	-	4	uA
Card supply voltage: pin CVCC						
CVCC	Supply voltage	5 V card; DC I _{CC} < 65 mA	4.75		5.25	V
		3 V card; DC I _{CC} < 65 mA	2.85	-	3.15	V
		1.8 V card; DC I _{CC} < 35 mA	1.71	-	1.89	V
I _{CC}	Drive current	CVCC = 5 V or 3 V	-	-	65	mA
		CVCC = 1.8 V	-	-	35	mA
Others						
T _{amb}	Operating temperature		-40	-	+85	°C

1.6 Pin Definition

Table 2. Definition of Mh1235h Chip Pin

Symbol	Pin	Supply	Type	Description
I/OUC	1	VDD	I/O	Main control data I/O line (internal 10K Ω pull-up resistor connected to VDD)
PORADJ	2	VDD	I	External resistance bridge
CMDVCCN	3	VDD	I	CVCC enable pin (efficient at low level)
VDD	4	VDD	supply	Interface power supply voltage
CLKDIV1	5	VDD	I	CLK frequency selection with CLKDIV2 control
CLKDIV2	6	VDD	I	CLK frequency selection with CLKDIV1 control
EN_5V/3VN	7	VDD	I	When EN_1.8 VN = high, and the pin signal is high, CVCC = 5V; and if the pin signal is low, CVCC = 3V.
EN_1.8 VN	8	VDD	I	When pin signal is low, CVCC = 1.8 V
RSTIN	9	VDD	I	Card reset input from host (efficient at high level)
OFFN	10	VDD	O	Interrupt signal detection
GND	11	-	supply	Ground connection
XTAL1	12	VDD	I	XTAL IN
XTAL2	13	VDD	O	XTAL OUT
VREG	14	VDDP	supply	External 0.1uF capacitor grounding
SAM	15	VDDP	I/O	DC-DC converter capacitor; connect between SAM and SAP; C = 330nF
GNDP	16	-	supply	Chip ground
SBM	17	VDDP	I/O	DC-DC converter capacitor; connect between SBM and SBP; C = 330nF

Symbol	Pin	Supply	Type	Description
VDDP	18	VDDP	supply	Supply voltage
SBP	19	VDDP	I/O	DC-DC converter capacitor; connect between SBM and SBP; C = 330nF
SAP	20	VDDP	I/O	DC-DC converter capacitor; connect between SAM and SAP; C = 330nF or 100nF
VUP	21	VDDP	I/O	DC-DC converter output decoupling capacitor connected between VUP and GNDC; C = 1uF
CVCC	22	CVCC	O	Card (C1) power supply pin
CRST	23	CVCC	O	Card end reset (C2)
CCLK	24	CVCC	O	Card end clock (C3)
GNDC	25	-	supply	Chip ground
CAUX1	26	CVCC	I/O	Card end auxiliary data line (C4), internal 10K Ω pull-up resistor connected to CVCC
CAUX2	27	CVCC	I/O	Card end auxiliary data line (C8), internal 10K Ω pull-up resistor connected to CVCC
CI/O	28	CVCC	I/O	Card end data line (C7), internal 10K Ω pull-up resistor connected to CVCC
CS	29	VDD	I	Host Chip Select Input (efficient at high level)
PRESN	30	VDD	I	Card detection contact input (efficient at low level); if PRESN is active, the card is considered to be present. Built-in typical 9 ms debounce function.
AUX1UC	31	VDD	I/O	Host's auxiliary data line, internal 10K Ω pull-up resistor connected to VDD
AUX2UC	32	VDD	I/O	Host's auxiliary data line, internal 10K Ω pull-up resistor connected to VDD

1.7 Packaging Information

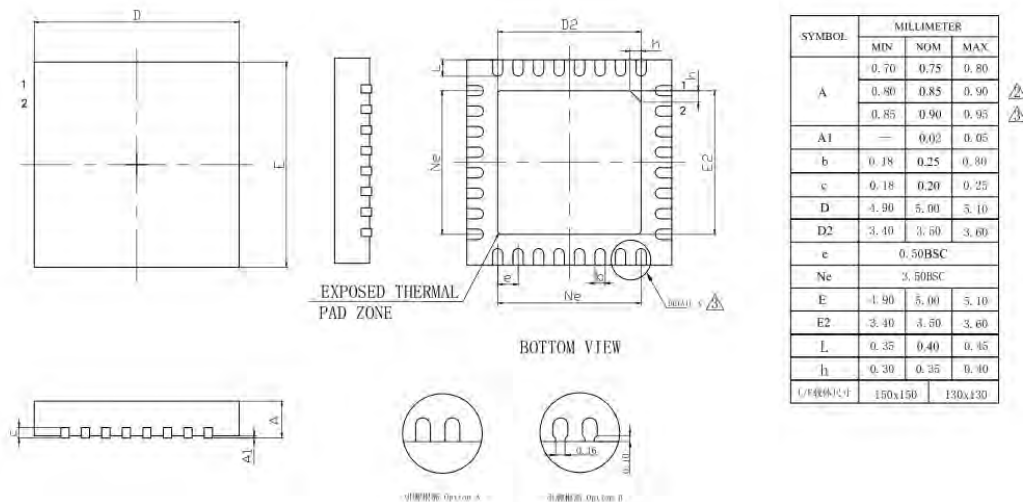


Figure 2. Dimensions of MH1235H Package

2. Function Module

2.1 Power

The power voltage VDDP is 2.7 V to 5.5 V.

The connection interface signals between the master control and MH1235H are all based on VDD.

After the chip is powered on, OFFN remains low until it detects that PRESN is low. At this time, it is considered that the card present, and OFFN will be pulled high.

When the power is off, OFFN drops to low level when the VDDP is lower than the threshold voltage.

The chip includes a DC-DC converter for generating a 5V, 3V, or 1.8V power supply voltage (CVCC). DC-DC converter power is provided by VDDP and GNDP separately.

2.2 Clock Circuit

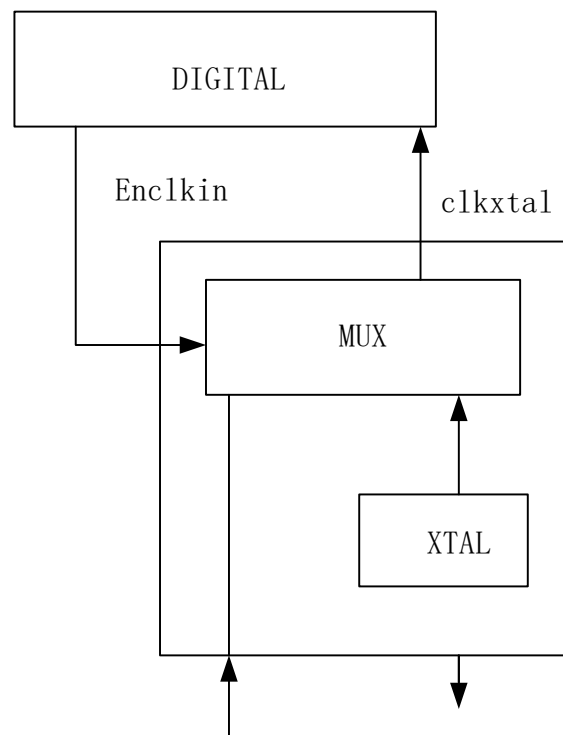


Figure 3. Switching the External Clock

To generate the card clock CLK, the MH1235H can use an external clock provided on the XTAL1 pin or a crystal oscillator connected on the XTAL1 and XTAL2 pins. The MH1235H will automatically detect when an external clock is available on XTAL1.

Therefore, no additional pins are required to configure the clock source (external clock or crystal oscillator).

Each activation command (falling edge of the CMDVCCN pin) performs automatic clock source detection. Check if an external clock is present on the XTAL1 pin. If a clock is detected, the crystal oscillator remains stopped; otherwise, the crystal oscillator is started. When using an external clock, the clock must be applied to XTAL1 before the CMDVCCN falling edge signal.

There is a delay circuit inside the card clock signal. When the falling edge of the CMDVCCN pin is detected, the delay circuit takes effect, and the delay time is about 4ms. After the delay release, if the input clock already exists, the card clock signal is output. If the input clock is not detected at this time, it will wait for the input clock signal. When the input clock signal is detected, the card clock will be output by 1 clock cycle of the delayed input clock.

If the input clock stops inputting for more than about 30us, the chip will automatically close the card clock circuit.

The duty cycle of the clock is kept between 45%~55%.

The frequency is selected as f_{XTAL} , $f_{XTAL}/2$, $f_{XTAL}/4$ or $f_{XTAL}/8$ by pins CLKDIV1 and CLKDIV2. The configuration method is shown in the following table:

Table 3. Clock Frequency Configuration

CLKDIV1	CLKDIV2	CLK
0	0	$f_{XTAL}/8$
0	1	$f_{XTAL}/4$
1	1	$f_{XTAL}/2$
1	0	f_{XTAL}

2.3 CS Control Circuit

The CS (Chip Select) input allows multiple chips to work in parallel. When CS is high, the system interface signals operate as described. When CS is low, the signals CMDVCCN, RSTIN, CLKDIV1, CLKDIV2, EN_5V / 3VN and EN_1.8VN are latched.

2.4 Shutdown Mode

The chip supports Shutdown Mode. After power-on reset, the CMDVCCN pin should be in a logic high state and cannot be left dangling. At this time, the chip is in Shutdown mode, waiting for the card insertion operation or the main control chip to control it.

2.5 Activation Timing

1. CMDVCCN is pulled low (t_0)
2. DC-to-DC starts $t_1 = t_0 + 1024 \times T_{osc}$
3. CVcc rises from 0 to selected CVcc value (5V, 3V, 1.8V) with a controlled slope ($t_2 = t_0 + 2048 \times T_{osc}$)
4. CI/O, CAUX1 and CAUX2 are enabled ($t_3 = t_0 + 3072 \times T_{osc}$), until now, they were pulled LOW
5. CCLK is applied to the C3 contact ($t_4 = t_0 + 3074 \times T_{osc}$)
6. CRST is enabled ($t_5 = t_0 + 3136 \times T_{osc}$).

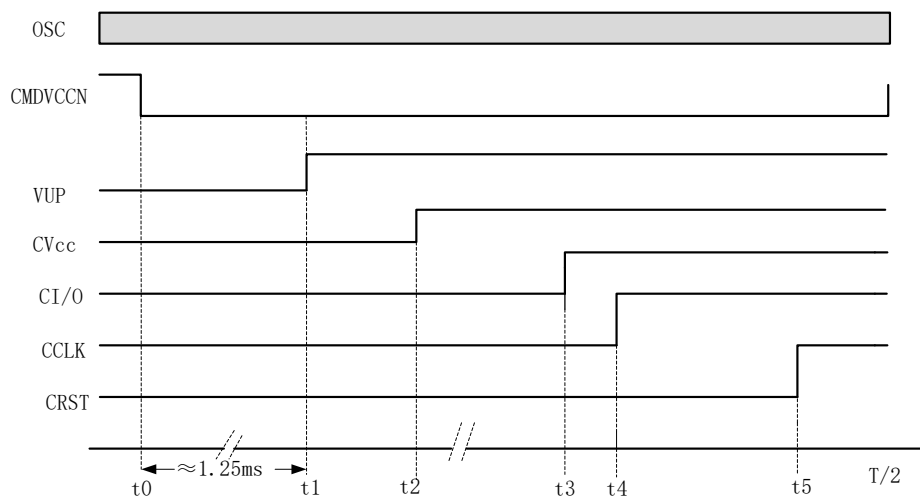


Figure 4. Activation Sequence

2.6 Inactivation Timing

1. CRST goes LOW ($t_{11} = t_{10} + 2 \times T_{osc}$)
2. CCLK is stopped LOW ($t_{12} = t_{10} + 12 \times T_{osc}$)
3. CI/O, CAUX1 and CAUX2 are pulled LOW ($t_{13} = t_{10} + 28 \times T_{osc}$)
4. CVcc falls to zero ($t_{14} = t_{10} + 38 \times T_{osc}$). The deactivation sequence is completed when CVcc reaches its inactive state.
5. VUP falls to zero ($t_{15} = t_{10} + 88 \times T_{osc}$)
6. All card contacts become low-impedance to GND. I/OUC, AUX1UC and AUX2UC remain pulled up to V_{DD} via a 10 k Ω resistor.
7. The internal oscillator reverts to its lower frequency.

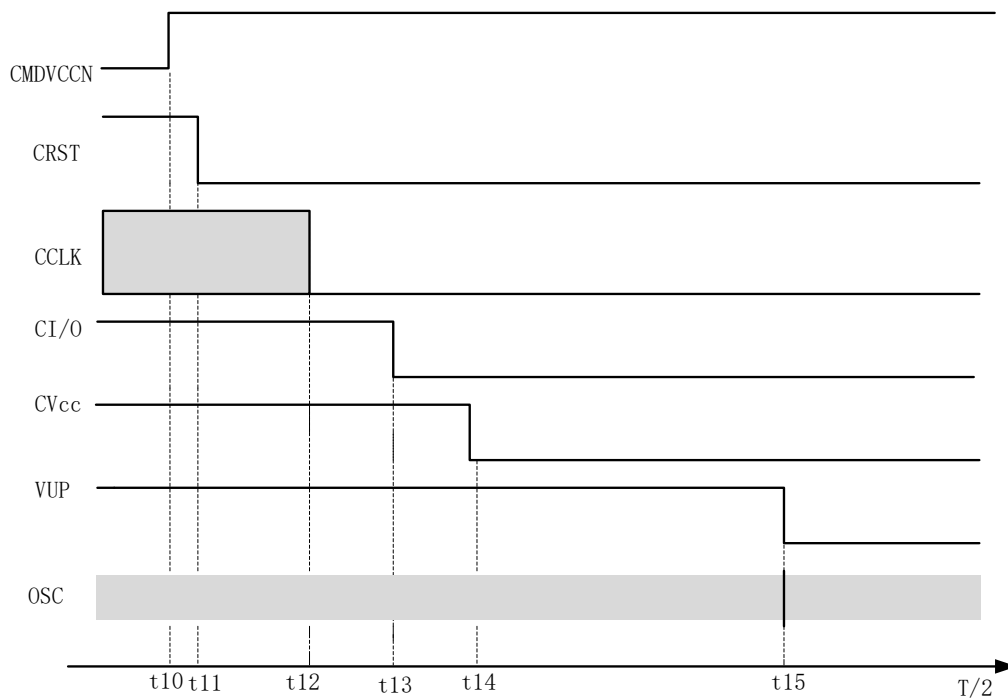


Figure 5. Deactivation Timing

2.7 Card end Voltage CVCC

CVCC can provide up to 65 mA continuously at CVCC = 5 V and CVCC = 3 V, and 35 mA at CVCC = 1.8 V.

CVCC has an internal overload detection function of about 130 mA. When the load current on CVCC is greater than 130mA or so, the chip will automatically power down.

The detection is filtered internally, allowing parasitic current pulses of up to 300 mA stuck around 500us without causing an outage.

2.8 Fault Detection

The chip detects the following fault conditions:

- Short circuit or overcurrent on CVCC
- Remove card during transaction
- VDDP is powered off
- Over-temperature

Here are two different applications

When CMDVCCN is high (no communication between card and MCU), OFFN is high when a card is inserted, and OFFN is low when no card is inserted. When VDDP is disconnected, OFFN is not affected, and the card end is not powered on, so there is no need to check for short circuit or overcurrent.

When CMDVCCN is low (during the communication between the card and MCU), OFFN will be set low in the above fault state. Once a fault condition is detected, the chip will automatically perform an emergency power down and power down according to the power down sequence. When the main control chip sets CMDVCCN high, OFFN status will be detected again.

During the card insertion or removal, due to mechanical reasons such as card slot, the PRESN signal may jitter. The chip supports the dithering function internally, and the dithering time is about 9ms.

3. Application Circuit

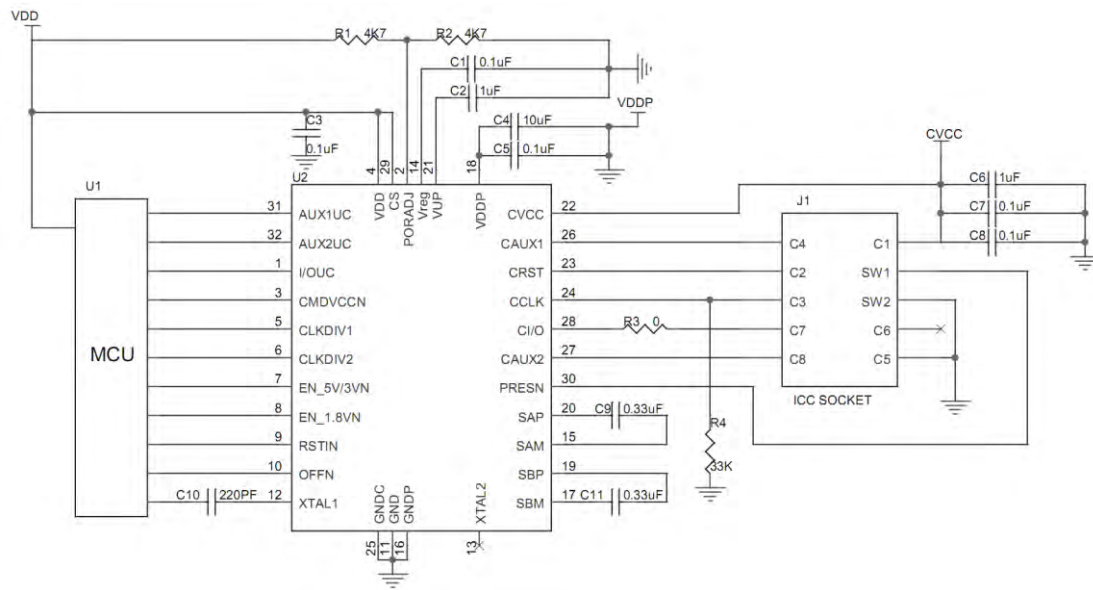


Figure 6. Reference Schematic

Precautions:

1. If using MCU clock, the accuracy of C10 capacitor should be guaranteed within 10%.
2. For EMVL1 certification related tests, it is recommended to reserve a pull-down resistor position on the CCLK pin at the card end, with a resistance value of 33K ~ 51K, and reserve a resistor at the CI/O pin.

4. Limit Value

All card-side pins have short-circuit protection between each other.

Exceeding the limit will permanently damage the chip.

Table 4. Limit Values

Symbol	Parameter	Conditions	Min	Max	Unit
VDDP	Supply voltage		-0.3	6	V
VDD	Interface power supply voltage		-0.3	4.1	V
VIH	High level input voltage	CS, PRESN, _____ CMDVCCN, CLKDIV2, CLKDIV1, EN_1.8VN, EN_5V/3VN, RSTIN, OFFN, PORADJ, XTAL1, I/OUC,AUX1UC,AUX2UC, VDDP, VDD	-0.3	4.1	V
		CI/O,CRST,CAUX1, CAUX2 and CCLK	-0.3	5.75	V
Vesd	Electrostatic parameter	Card end pin CI/O, CRST, CCLK, CAUX1, CAUX2, CVCC, PRESN	-8	+8	KV
Tamb	Ambient temperature		-40	+85	°C
Tstg	Storage temperature		-55	+150	°C

5. Electrical Characteristics

Table 5. Chip Characteristics

$V_{DDP} = 3.3V$; $V_{DD} = 3.3V$; $f_{XTAL} = 4MHz$; $GND = 0V$; $T_{amb} = 25^{\circ}C$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
VDDP	Supply voltage		2.7	3.3	5.5	V
VDD	Interface power supply voltage		1.6	3.3	3.6	V
I _{DDP}	Supply current	shutdown mode; f _{XTAL} = stopped;	-	-	180	uA
		active mode; CVCC =+5 V CLK = f _{XTAL} ; no load	-	-	5	mA
		active mode; CLK = f _{XTAL} ; CVCC = +5 V; I _{CC} = 65 mA	-	-	140	mA
		active mode; CLK = f _{XTAL} ; CVCC = +3 V; I _{CC} = 65 mA	-	-	140	mA
		active mode; CLK = f _{XTAL} ; CVCC = +1.8V; I _{CC} = 35 mA	-	-	80	mA
I _{DD}	Interface supply current	shutdownmoe; f _{XTAL} =stopped; presentcard	-	-	4	uA
VUP (DC-DC transverter)						
V _{up}	Output voltage	VDDP=3.3V,CVCC=5V,I _{cc} <65mA	5.2		5.4	V
		VDDP=3.3V,CVCC=3V,I _{cc} <65mA	5.2		5.4	V
		VDDP=3.3V,CVCC=1.8V,I _{cc} <35mA	5.2		5.4	V
		VDDP=5V,CVCC=5V,I _{cc} <65mA	5.2		5.4	V
		VDDP=5V,CVCC=3V,I _{cc} <65mA	5.2		5.4	
		VDDP=5V,CVCC=1.8V,I _{cc} <35mA	5.2		5.4	
DC-to-DC converter capacitor						
CSAPSAM	DC/DC converter capacitor	connected between SAP and SAM (330 nF) with VDDP=3.3v	231	-	429	nF
		connected between SAP and SAM (100 nF) with VDDP=5v	70	-	130	nF
CSBPSBM	DC/DC converter capacitor	connected between SBP and SBM (330 nF) with VDDP=3.3v	231	-	429	nF
		connected between SBP and SBM (100 nF) with VDDP=5v	70	-	130	nF
CVUP	DC/DC converter capacitor	connected on VUP	700	-	1300	nF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Card supply voltage (CVCC)						
Cdec	Decoupling capacitor	connected on CVCC (1uF + 100nF+100nF 10 %)	440	-	4700	nF
Io	Current output	inactive mode at grounded pin CVCC	-	-	-1	mA
CVCC	Supply voltage	active mode; 5 V card; ICC < 65 mA DC	4.95	5.0	5.25	V
		active mode; 3 V card; ICC < 65 mA DC	2.85	3.05	3.15	V
		active mode; 1.8 V card; ICC < 35 mA DC	1.71	1.83	1.89	V
		active mode; current pulses of 40 nA/s with ICC < 200 mA, t< 400 ns; 5V card	4.75	5.0	5.25	V
		active mode; current pulses of 40 nA/s with ICC < 200 mA, t< 400 ns; 3V card	2.76	-	3.20	V
		active mode; current pulses of 15 nA/s with ICC < 200 mA, t < 400 ns; 1.8 V card	1.66	-	1.94	V
Vripple(p-p)	Peak-to-peak ripple voltage	from 20 kHz to 200 MHz	-	-	350	mV
ICC	Supply current	CVCC = 0 V to 5 V, 3 V	-	-	65	mA
		CVCC = 0 V to 1.8 V	-	-	35	mA
SR	Conversion rate	5 V card	0.055	0.18	0.8	V/s
		3 V card	0.040	0.18	0.8	V/s
		1.8 V card	0.025	0.18	0.8	V/s
Crystal oscillator (XTAL1 and XTAL2)						
Cext	External capacitance	Connect XTAL1, XTAL2 (Select the capacitor size according to the specifications of the external crystal)	-	-	33	pF
fxtal	Crystal frequency		2	-	27	MHz
fxtal(XTAL1)	Crystal frequency on pin XTAL1	Series 220pF capacitor	0	-	27	MHz
VIL	Low level input voltage		-0.3	-	+0.3VDD	V
VIH	High level input voltage		0.7VDD	-	VDD+0.3	V
tr(i)	Input rise time	fCLK = fXTAL1 = 20 MHz on external clock	-	-	5	ns
		fCLK = fXTAL1 = 10 MHz on external clock	-	-	5	ns
		fCLK = fXTAL1 = 5 MHz on	-	-	5	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		external clock				
tf(i)	Input fall time	fCLK = fXTAL1 = 20 MHz on external clock	-	-	6	ns
		fCLK = fXTAL1 = 10 MHz on external clock	-	-	6	ns
		fCLK = fXTAL1 = 5 MHz on external clock	-	-	6	ns
Data cable (pinsC I/O, I/OUC, CAUX1, CAUX2, AUX1UC, AUX2UC)						
td	Delay time	falling edge on pins I/O and I/OUC or I/OUC and I/O		-	200	ns
tw(pu)	Pull-up pulse width		200		400	ns
fmax	Maximum frequency	on data lines	-	-	1	MHz
Ci	Input capacitance	on data lines	-	-	10	pF
Card end data cable (pinsC I/O,CAUX1,CAUX2); (Integrated 10kΩ pull-up resistor connected to CVcc)						
Vo	Output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; Io= 1 mA	0	-	0.3	V
Io	Output current	inactive mode at grounded pin I/O	-	-	1	mA
VOL	Low-level output voltage	IOL =1 mA	0	-	0.3	V
		IOL≥15 mA	CVCC-0.4	-	CVCC	V
VOH	High-level output voltage	No DC load	0.9CVCC	-	CVCC +0.1	V
		IOH < -40 uA 5 V or 3 V	0.75CVCC	-	CVCC +0.1	V
		IOH < -20 uA 1.8 V	0.75CVCC	-	CVCC +0.1	V
		IOH ≥-15 mA	0	-	0.4	V
VIL	Low-level input voltage		-0.3	-	+0.8	V
VIH	High-level input voltage	CVCC = +5 V	0.6CVCC	-	CVCC+0.3	V
		CVCC = +3 V or 1.8 V	0.7CVCC	-	CVCC+0.3	V
Vhys	Lagging voltage	on I/O	30	75	120	mV
IIL	Low-level input voltage	on I/O; VIL = 0	-	-	600	uA
ILH	High-level leakage current	on I/O; VIH = CVCC	-	-	10	uA
tr(i)	Input rise time	from VIL max to VIH min	-	-	50	ns
tf(i)	Input fall time	from VIL max to VIH min	-	-	50	ns
tr(o)	Output rise time	CL <= 80 pF; 10 % to 90 % from 0 to CVCC	-	-	50	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
tf(o)	Output fall time	CL <= 80 pF; 10 % to 90 % from 0 to CVCC	-	-	50	ns
Rpu	Pull-up resistor	connected to CVCC	8	10	12	KΩ
Ipu	Pull-up current	VOH = 0.9 CVCC, C = 80 pF	-8	-6	-4	mA
Data lines to the system; pins I/OUC, AUX1UC, AUX2UC						
VOL	Low level output voltage	IOL =1 mA	0	-	0.3	V
VOH	High level output voltage	No DC load	0.9 VDD	-	VDD+0.1	V
		IOH≤40uA; VDD >2 V	0.75VDD	-	VDD+0.1	V
		IOH ≤20 uA; VDD <2 V	0.75VDD	-	VDD+0.1	V
VIL	Low level input voltage		-0.3	-	0.3VDD	V
VIH	High level input voltage		0.7 VDD	-	VDD+0.3	V
Vhys	Lagging voltage	on I/Ouc	0.05VDD	-	0.25VDD	V
ILH	High level leakage current	VIH = VDD			10	uA
IIL	Low level input current	VIL = 0			600	uA
Rpu	Pull-up resistor	connected to VDD	8	10	12	KΩ
tr(i)	Input rise time	from VIL max to VIH min	-	-	1.2	us
tf(i)	Input fall time	from VIL max to VIH min	-	-	1.2	us
tr(o)	Output rise time	CL≤30 pF; 10 % to 90 % from 0 to VDD	-	-	0.1	us
tf(o)	Output fall time	CL≤30 pF; 10 % to 90 % from 0 to VDD	-	-	0.1	us
Ipu	Pull-up current	VOH = 0.9 VDD, C = 30 pF	-1	-	-	mA
Internal oscillator						
fosc(int)	Internal oscillation frequency	inactivestate: osc(int)_Low	230	315	430	kHz
		active state: osc(int)_High	2.0	2.5	3.0	MHz
Card end reset (CRST)						
Vo	Output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; Io= 1 mA	0	-	0.3	V
Io	Output current	inactive mode at grounded pin RST	-	-	-1	mA
td	Delay time	between RSTIN and RST, RST enabled	-	-	200	ns
VOL	Low level output	IOL= 200 uA, CVCC = +5 V	0	-	0.3	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	voltage	IOL = 200 uA, CVCC = 3V or 1.8V	0	-	0.2	V
		IOL = 20 mA (current limit)	CVCC-0.4	-	CVCC	V
VOH	High level output voltage	IOH = -200 mA	0.9CVCC	-	CVCC	V
		IOH = -20 mA (current limit)	0	-	0.4	V
tr	Rise time	CL = 100 pF CVCC = +5 V and +3 V	-	-	0.1	us
		CL = 100 pF CVCC = +1.8 V	-	-	0.2	us
tf	Fall time	CL = 100 pF CVCC = +5 V and +3 V	-	-	0.1	us
		CL = 100 pF CVCC = +1.8 V	-	-	0.2	us
Card end clock (CCLK)						
Vo	Output voltage	inactive mode; no load	0	-	0.1	V
		inactive mode; Io = 1 mA	0	-	0.3	V
Io	Output current	inactive mode at grounded pin CLK	-	-	-1	mA
VOL	Low level output voltage	IOL = 200 uA	0	-	0.3	V
		IOL = 70 mA (current limit)	CVCC-0.4	-	CVCC	V
VOH	High level output voltage	IOH = -200 uA	0.9CVCC	-	CVCC	V
		IOH = -70 mA (current limit)	0	-	0.4	V
tr	Rise time	CL = 30 pF	-	-	16	ns
tf	Fall time	CL = 30 pF	-	-	16	ns
fCLK	Frequency at pin clk	Operational	0	-	20	MHz
	Duty cycle	CL = 30 pF [2]	45	-	55	%
SR	Conversion rate	rise and fall; CL = 30 pF; CVCC = +5 V	0.2	-	-	V/ns
		rise and fall; CL = 30 pF; CVCC = +3 V	0.12	-	-	V/ns
		rise and fall; CL = 30 pF; CVCC = +1.8 V	0.072	-	-	V/ns
Control Input (pins CS, CMDVCCN, CLKDIV1, CLKDIV2, RSTIN, EN_5V/ 3VN, EN_1.8VN)						
VIL	Low level output voltage		-0.3	-	+0.3VDD	V
VIH	High level output voltage		0.7 VDD	-	VDD+0.3	V
Vhys	Lagging voltage	on control input	0.05VDD	-	0.25VDD	V
ILL	Low level leakage current	VIL = 0	-	-	1	uA
ILH	High level leakage current	VIH = VDD	-	-	1	uA
Card presence input (PRESN); PRESN has an integrated pull down resistor [3]						

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIL	Low-level input voltage		-0.3	-	+0.3VDD	V
VIH	High-level input voltage		0.7 VDD	-	VDD+0.3	V
Vhys	Hysteresis voltage		0.05VDD	-	0.10 VDD	V
ILL	Low-level leakage current	VIL = 0	-	-	1	uA
ILH	High-level leakage current	VIH = VDD	-	-	5	uA
OFFN output (pin OFFN is an NMOS drain with a 10k pull-up resistor to VDD)						
VOL	Low-level output voltage	IOL =2 mA	0	-	0.3	V
VOH	High-level output voltage	IOH = -15 uA	0.75VDD	-		V
Rpu	Pull-up resistor		8	10	12	KΩ
Protection and restriction						
Tsd	Over temperature		-	150	-	°C
IOlim	Output current limit	on pin I/O	-15	-	+15	mA
		on pin CLK	-70	-	+70	mA
		on pin RST	-20	-	+20	mA
		on pin CVCC = 5 V or 3 V	90	125	160	mA
		on pin CVCC = 1.8V	90	130	160	mA
Isd	Overcurrent	on pin CVCC = 5 V or 1.8 V	80	115	300	mA
		on pin CVCC = 3 V	80	150	250	mA
Timing						
tact	Activation time		1847	-	3390	us
tdeact	Inactive time		35	90	250	us
tact	Activation time	time of the window for sending CLK to the card with XTAL1	1992	2690	3653	us
			2055	2766	3749	us
tdeb	Debounce time	on pin PRESN			10	ms