FORESEE®

192Mbit SPI NAND Flash

F35SQA192M

Datasheet

LM-00452

Rev 0.1

Revision History

Rev.	Date	Changes
0.1	2025/8/22	Preliminary

Content

1 General Description

The F35SQA192M is a 192M-bit (24Mx8bit) Serial NAND Flash Memory, operates on a single 3.3V VCC. The device supports the standard Serial Peripheral Interface (SPI), Dual/Quad SPI: Serial Clock, Chip Select, Serial Data SIO0 (DI), SIO1 (DO), SIO2 (WP#) and SIO3 (HOLD#).

The F35SQA192M supports JEDEC standard manufacturer and device ID, Unique ID, one parameter page and 62 OTP pages. An internal 1-bit ECC logic is available in the chip, which is enabled by default. The internal ECC can be disabled or enabled by command.

2 Features

Voltage Supply
- VCC: 2.7V ~ 3.6V

Organization
- Memory Cell Array: (24M + 768k) Byte
- Page Size: (2k + 64) Byte
- Block Size: 64 pages, (128k + 4k) Byte

Serial Interface
- Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
- Dual SPI: CLK, CS#, SIO0-SIO1, WP#, HOLD#
- Quad SPI: CLK, CS#, SIO0-SIO3

High Performance
- 166 MHz Standard/Dual/Quad SPI clocks
- 83 MHz DTR Read SPI clock
- Page Program Time: 350μs (Typ.)
- Block Erase Time: 2ms (Typ.)

Low Power
- Standby: 10μA (Typ.)
- Page Read: 10mA (Typ.)
- Program/Erase: 15mA (Typ.)

Advanced Features
- Support Continuous and Sequential Read
- On chip 1-Bit ECC for memory array
- Software and Hardware write protect
- Bad Block Management and LUT access
- Unique ID
- One 2kB parameter page
- Sixty-two 2kB OTP Pages
- Promised golden block0

High Reliability
- Endurance: typical 100k cycles (1)
- Data Retention: 20 years (1)

Package
- 8-WSON (5x6mm)
- 8-SOP (208mil)
- 8-SOP (150mil)

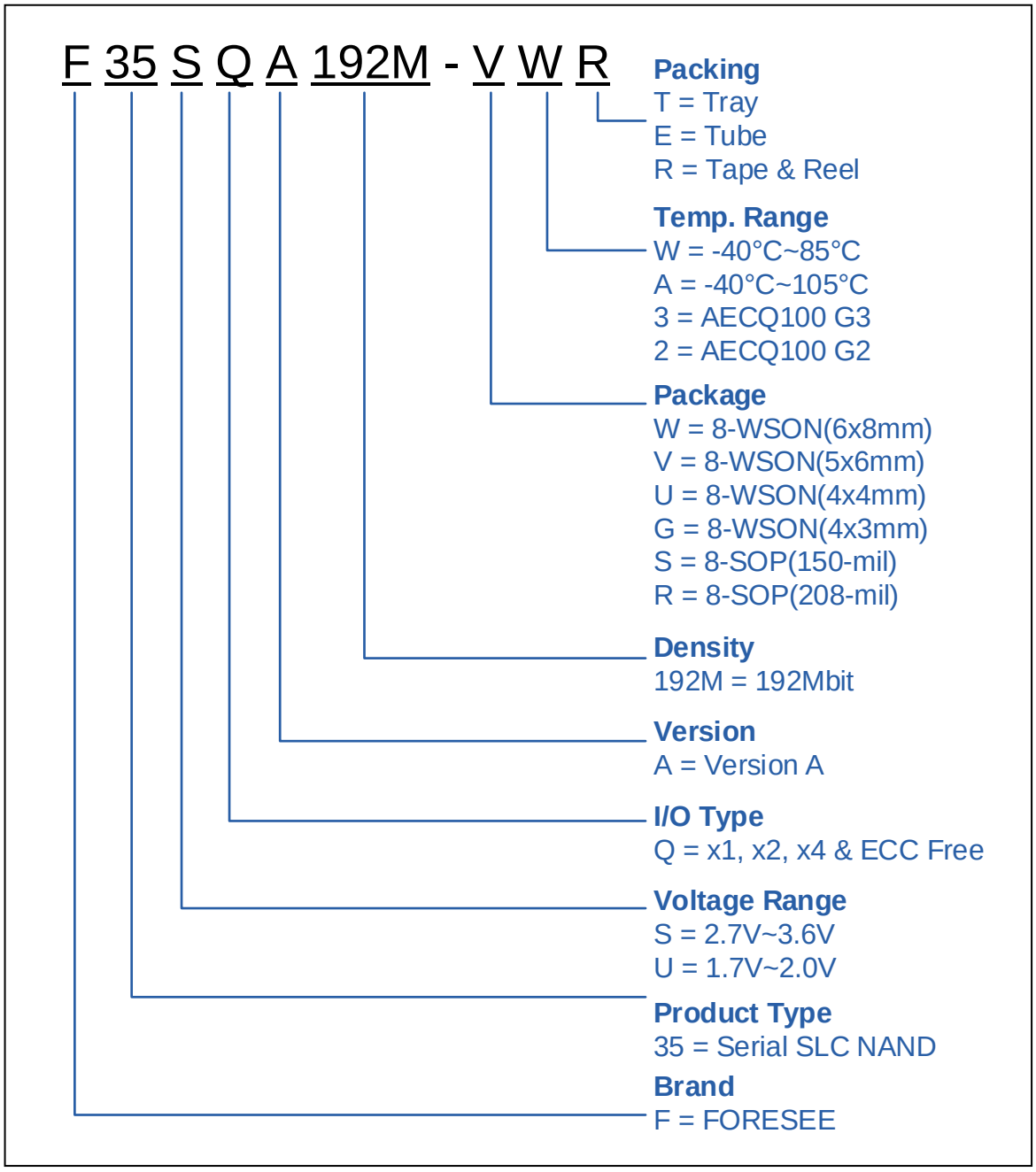
Note:
(1) Endurance and Data Retention specification is based on 1bit / 528Byte ECC

3 Product List

Table 1 Product List

Part Number	Density	I/O Type	Voltage Range	Package	Temp. Range	Packing
F35SQA192M-VWR	192Mb	x1, x2, x4	2.7V ~ 3.6V	8-WSON (5x6mm)	-40°C ~ 85°C	T&R
F35SQA192M-RWR	192Mb	x1, x2, x4	2.7V ~ 3.6V	8-SOP (208-mil)	-40°C ~ 85°C	T&R
F35SQA192M-RWE	192Mb	x1, x2, x4	2.7V ~ 3.6V	8-SOP (208-mil)	-40°C ~ 85°C	Tube
F35SQA192M-SWR	192Mb	x1, x2, x4	2.7V ~ 3.6V	8-SOP (150-mil)	-40°C ~ 85°C	T&R
F35SQA192M-SWE	192Mb	x1, x2, x4	2.7V ~ 3.6V	8-SOP (150-mil)	-40°C ~ 85°C	Tube

Figure 1 Marketing Part Numbering Chart



4 Package Types and Pin Configurations

Figure 2 Pin Configuration 8-WSON

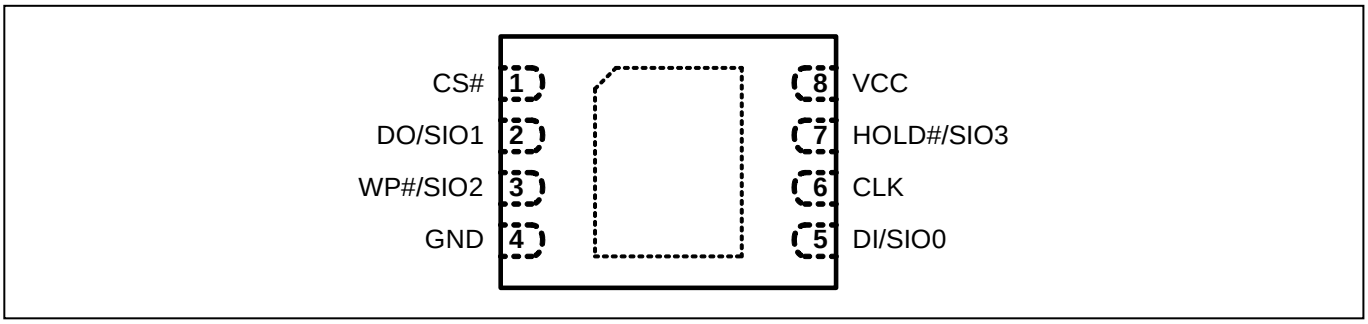
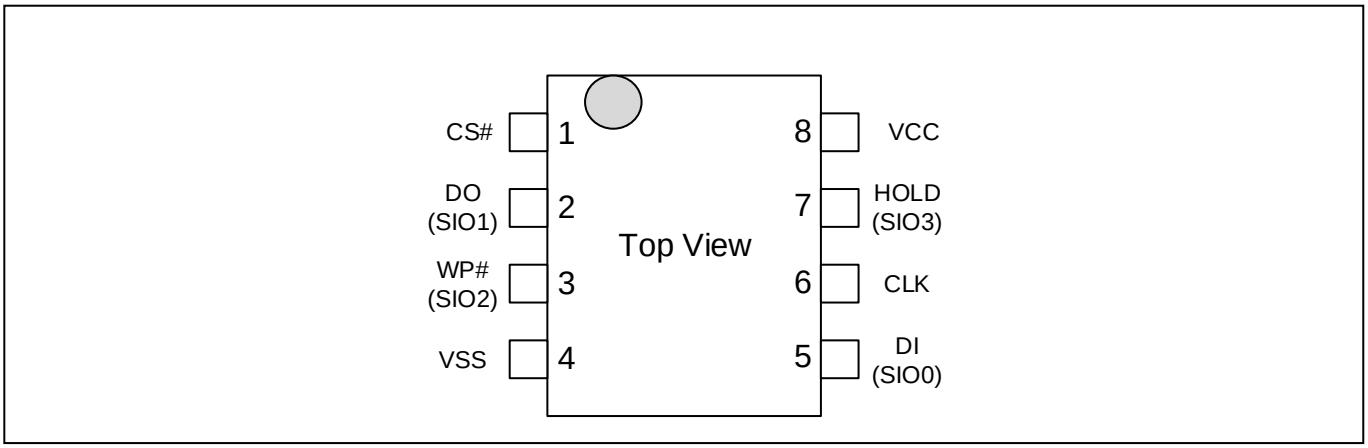


Figure 3 Pin Configuration 8-SOP



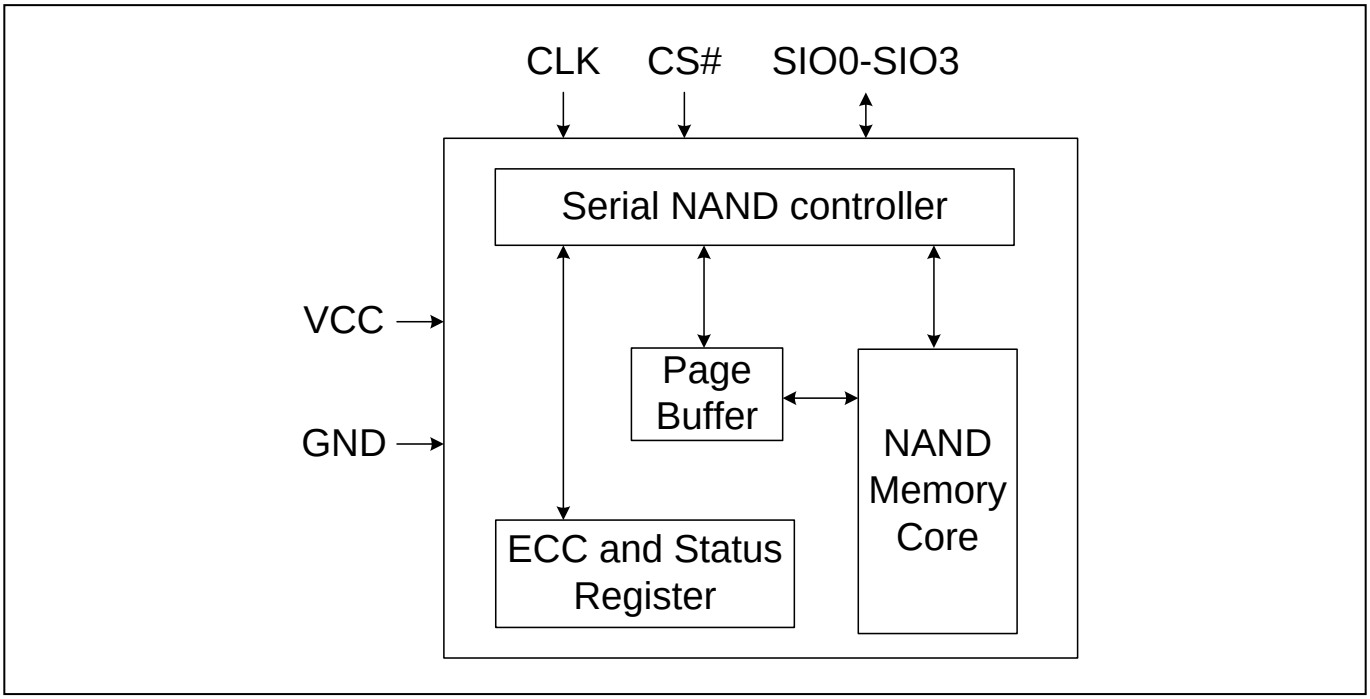
5 Pin Descriptions

Table 2 Pin Description

Pin Name	Pin Functions
CS#	**Chip Select** The SPI Chip Select pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO or SIO0-3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.
DI, DO and SIO0-SIO3	**Serial Data Input, Output and IOs** The device supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK. Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.
WP#	**Write Protect** The WP# pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect bits (BP3-0, TB) and Status Register Protect bits (BPRWD, SP), a portion as small as 128k-Byte (1 block) or up to the entire memory array can be hardware protected.
HOLD#	**Hold** During Standard and Dual SPI operations, the HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When HOLD# is brought high, device operation can resume. The HOLD function can be useful when multiple devices are sharing the same SPI signals. The HOLD# pin is active low. When a Quad SPI Read/Program Data Load command is issued, HOLD# pin will become a data I/O pin for the Quad operations and no HOLD function is available until the current Quad operation finishes.
CLK	**Serial Clock** The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations.
GND	**Ground**
VCC	**VCC** Power Supply
NC	**No Connection**

6 Block Diagram

Figure 4 Block Diagram



7 Array Organization and Mapping

Figure 5 Array Organization

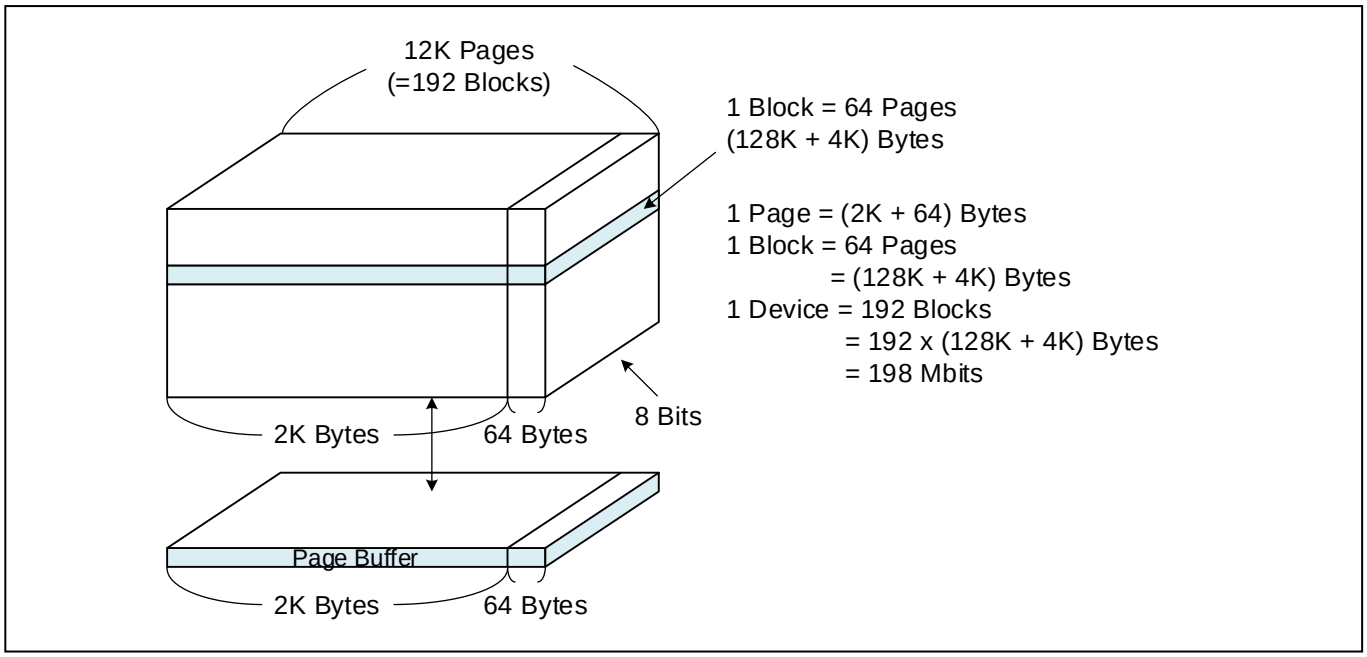
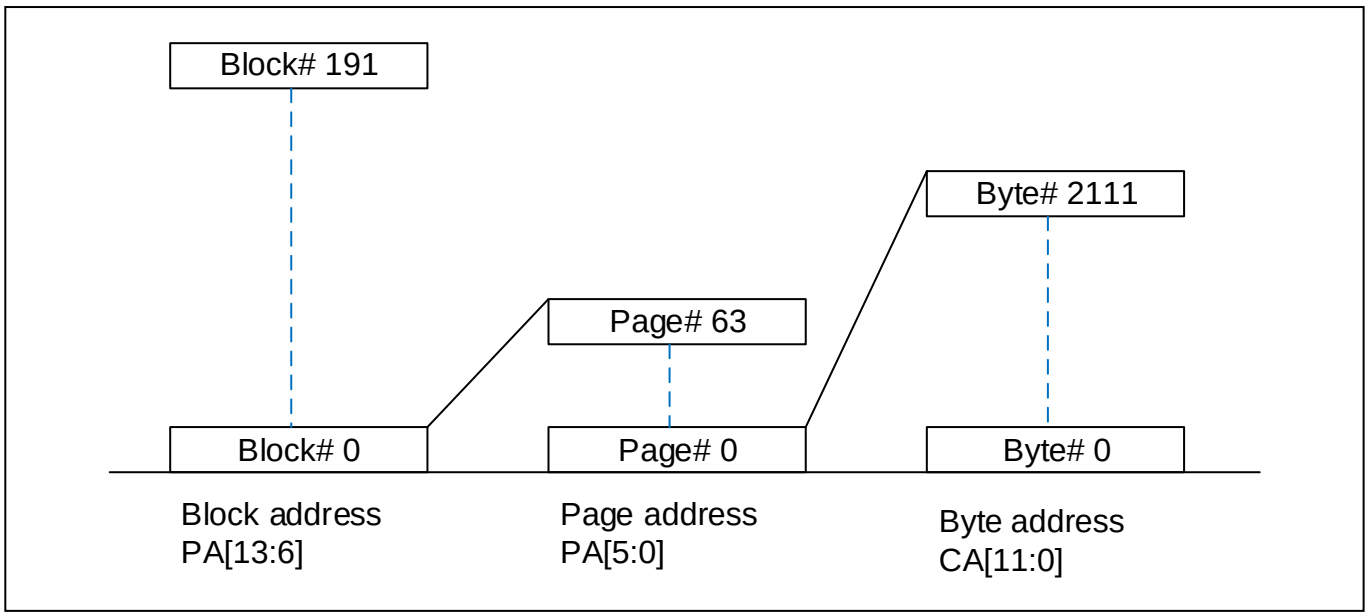


Figure 6 Address Mapping



Note:

1. The 12-bit byte address is capable of addressing from 0 to 4095 bytes. However, only bytes 0 through 2111 are valid, the rests are “out of bounds” and cannot be addressed.

8 Device Operation

8.1 General

1. Before a command is issued, status register should be checked via get feature operations to ensure device is ready for the intended operation.
2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SIO pin of this device should be High-Z.
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.

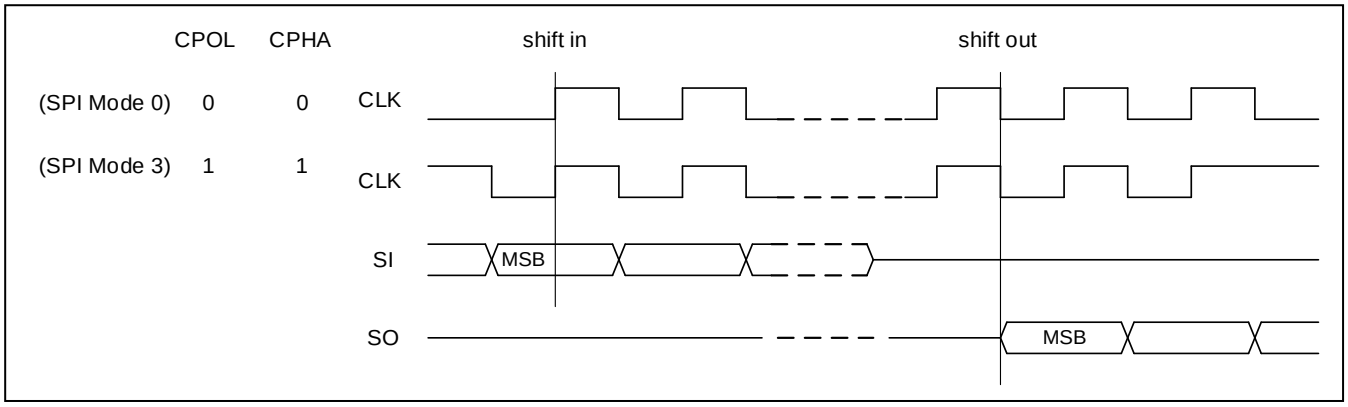
8.2 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched on the rising edge of CLK and data shifts out on the falling edge of CLK for both modes. All timing diagrams shown in this data sheet are mode 0. The difference of Mode 0 and Mode 3 is shown as **Figure 7**.

Figure 7 SPI Mode Supported



Standard SPI

SPI NAND Flash features a standard serial peripheral interface on 4 signals bus: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO).

Dual SPI

SPI NAND Flash supports Dual SPI operation when using the x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the DI and DO pins become bidirectional I/O pins: SIO0 and SIO1.

Quad SPI

SPI NAND Flash supports Quad SPI operation when using the x4 and Quad IO commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the DI and DO pins become bidirectional I/O pins: SIO0 and SIO1, and WP# and HOLD# pins become SIO2 and SIO3.

DTR Read

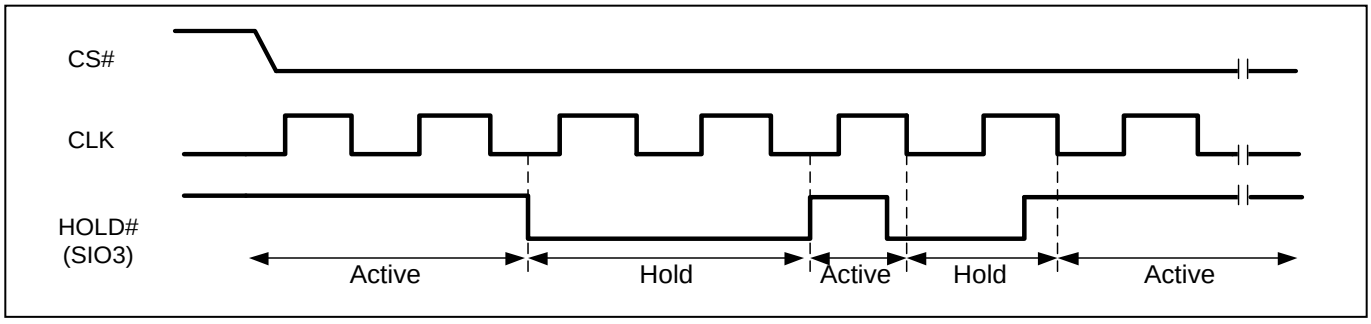
To effectively improve the read operation throughput without increasing the serial clock frequency, the device introduces DTR (Double Transfer Rate) Read commands that support Standard/Dual/Quad SPI modes. The byte-long command code is latched into the device on the rising edge of the serial clock similar to all other SPI commands. Once a DTR command code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

8.3 Hold Function

For Standard SPI and Dual SPI operations, the HOLD# signal allows the device operation to be paused while it is actively selected (when CS# is low). The Hold function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the Hold function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again. The Hold function is only available for standard SPI and Dual SPI operation, not during Quad SPI or DTR operation. When a Quad SPI command is issued, HOLD# pin will act as a dedicated IO pin (SIO3).

To initiate a HOLD condition, the device must be selected with CS# low. A HOLD condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD condition will activate after the next falling edge of CLK. The HOLD condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD condition will terminate after the next falling edge of CLK. During a HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD operation to avoid resetting the internal logic state of the device. See **Figure 8** for more details.

Figure 8 Hold Condition



8.4 Write Protection

The device provides several means to protect the data from inadvertent writes.

- Device resets when VCC is below threshold
- Write enable/disable instructions and automatic write disable after erase or program
- Software and Hardware (WP# pin) write protection using Protection Register
- Lock Down write protection for Protection Register until the next power-up
- One Time Program (OTP) write protection for memory array using Protection Register

After power-up the device is automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Program Execute or Block Erase instruction will be accepted. After completing a program or erase instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (BPRWD, SP) and Block Protect (TB, BP3-0) bits. These settings allow a portion or the entire memory array to be configured as read only. Used in conjunction with the WP# pin, changes to the Status Register can be enabled or disabled under hardware control. See **Protection Register** for further information.

9 Status Registers

For Protection Register, Configuration Register and Status Register, each register is accessed by Get Feature (0Fh) and Set Feature (1Fh) commands combined with 1-Byte Register Address respectively.
For Sector ECC Status Registers, each one can only be accessed by Get Feature (0Fh) command combined with 1-Byte Register Address.

Table 3 Status Registers

Register	Address	Data Bits							
		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Protection	A0h	BPRWD	BP3	BP2	BP1	BP0	TB	R	SP
Configuration	B0h	OTP-L	OTP-E	R	ECC-E	R	DRV1	DRV0	QE
Status	C0h	R	LUT-F	ECCS1	ECCS0	P-FAIL	E-FAIL	WEL	OIP
Configuration	D0h	R	R	R	R	R	R	CONT	BUF
Configuration	E0h	R	R	R	DEFECC-E	R	R	DEFCONT	DEFBUF
Sector0 ECC Status	80h	S0_ECCS[7:0], Refer to Sector ECC Status							
Sector1 ECC Status	84h	S1_ECCS[7:0], Refer to Sector ECC Status							
Sector2 ECC Status	88h	S2_ECCS[7:0], Refer to Sector ECC Status							
Sector3 ECC Status	8Ch	S3_ECCS[7:0], Refer to Sector ECC Status							

Note:

(1) R: Reserved Bit and has no function. They are read out as “0”. It is recommended to ignore the values of those bits. During a Set Feature command, the Reserved Bits can be written as “0” or “1”, but there will not be any effects.

The Reset command (FFh) will not clear the previous feature setting, the feature setting data bits remain until the power is being cycled or modified by the settings in the table below. After a Reset command is issued, the OIP bit will go high. This bit can be polled to determine when the Reset operation is complete, as it will return to the default value (0) after the reset operation is finished. Issuing the Reset command has no effect on the Block Protection and Configuration registers.

Table 4 Default Values of the Status Registers after power up and Device Reset

Register	Address	Bits	Shipment Default	Power Up	After Reset Command
Protection	A0h	BP3-0, TB	1 1 1 1 1	1 1 1 1 1	No Change
		BPRWD	0	0	No Change
		SP	0	0	No Change
Configuration	B0h	OTP-L	0	Loked:1, else 0	No Change
		OTP-E	0	0	No Change
		ECC-E	1	User Define (1)	No Change
		QE	0	0	No Change

Register	Address	Bits	Shipment Default	Power Up	After Reset Command
		DRV1-0	0 0	0 0	No Change
Status	C0h	ECCS1-0	0 0	Status of Page0/Block0	0 0
		LUT-F	0	Status of LUT	No Change
		P-FAIL	0	0	0
		E-FAIL	0	0	0
		WEL	0	0	0
		OIP	0	0	0
Configuration	D0h	CONT	1	User Define (2)	No Change
		BUF	1	User Define (3)	No Change
Configuration	E0h	DEFECC-E	1	OTP write:0, else 1	No Change
		DEFCONT	1	OTP write:0, else 1	No Change
		DEFBUF	1	OTP write:0, else 1	No Change
Sector0 ECC Status	80h	S0_ECCS[7:0]	00h	Sector0 ECC Status of Page0/Block0	00h
Sector1 ECC Status	84h	S1_ECCS[7:0]	10h	Sector1 ECC Status of Page0/Block0	10h
Sector2 ECC Status	88h	S2_ECCS[7:0]	20h	Sector2 ECC Status of Page0/Block0	20h
Sector3 ECC Status	8Ch	S3_ECCS[7:0]	30h	Sector3 ECC Status of Page0/Block0	30h

Note:

(1) The Power Up default value can be changed **once** by write DEFECC-E bit. See ”Default value of ECC-E bit (DEFECC-E)”

(2) The Power Up default value can be changed **once** by write DEFCONT bit. See ”Default value of CONT bit (DEFCONT)”

(3) The Power Up default value can be changed **once** by write DEFBUF bit. See ”Default value of BUF bit (DEFBUF)”

9.1 Protection Register

9.1.1 Block Protect Bits (BP3-0, TB)

The Block Protect bits (BP3-0, TB) are volatile read/write bits that provide Write Protection control and status. Block Protect bits can be set using the Set Feature Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (See **Table 6**). The default values for the Block Protection bits are 1 after power up to protect the entire array.

9.1.2 Status Register Protect Bits (BPRWD, SP)

The Status Register Protect bits (BPRWD, SP) are volatile read/write bits which control the method of write protection: software protection, hardware protection, power supply lock-down.

Table 5 Status Register Protection

BPRWD	SP	QE	WP#	Descriptions
X	0	1	X	Protection Register can be changed No WP# functionality, WP# pin will always function as SIO2
X	1	X	X	Protection Register cannot be changed during the current power cycle
0	0	0	X	Protection Register can be changed
1	0	0	0	Protection Register can NOT be changed
1	0	0	1	Protection Register can be changed

Note:

(1) When SP =1, a power-down, power-up cycle will change (BPRWD, SP) to (0, 0) state.

9.1.3 Status Register Memory Protection

Table 6 Block Protection Bits

TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[13:0]	PROTECTED DENSITY
X	0	0	0	0	NONE	NONE	NONE
X	1	1	1	1	ALL	0000h - 27FFh	20MB
0	0	0	0	1	191	27C0h – 2FFFh	128kB
0	0	0	1	0	190 thru 191	2F80h – 2FFFh	256kB
0	0	0	1	1	188 thru 191	2F00h – 2FFFh	512kB
0	0	1	0	0	184 thru 191	2E00h – 2FFFh	1MB
0	0	1	0	1	176 thru 191	2C00h – 2FFFh	2MB
0	0	1	1	0	160 thru 191	2800h – 2FFFh	4MB
0	0	1	1	1	144 thru 191	2400h – 2FFFh	6MB
0	1	0	0	0	128 thru 191	2000h – 2FFFh	8MB
0	1	0	0	1	112 thru 191	1C00h – 2FFFh	10MB
0	1	0	1	0	96 thru 191	1800h – 2FFFh	12MB
0	1	0	1	1	80 thru 191	1400h – 2FFFh	14MB
0	1	1	0	0	64 thru 191	1000h – 2FFFh	16MB

TB	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED PAGE ADDRESS PA[13:0]	PROTECTED DENSITY
0	1	1	0	1	48 thru 191	0C00h – 2FFFh	18MB
0	1	1	1	0	32 thru 191	0800h – 2FFFh	20MB
0	1	1	1	1	ALL	0000h – 2FFFh	24MB
1	0	0	0	1	0	0000h – 003Fh	128kB
1	0	0	1	0	0 thru 1	0000h – 007Fh	256kB
1	0	0	1	1	0 thru 3	0000h - 00FFh	512kB
1	0	1	0	0	0 thru 7	0000h - 01FFh	1MB
1	0	1	0	1	0 thru 15	0000h - 03FFh	2MB
1	0	1	1	0	0 thru 31	0000h - 07FFh	4MB
1	0	1	1	1	0 thru 47	0000h – 0BFFh	6MB
1	1	0	0	0	0 thru 63	0000h – 0FFFh	8MB
1	1	0	0	1	0 thru 79	0000h - 13FFh	10MB
1	1	0	1	0	0 thru 95	0000h - 17FFh	12MB
1	1	0	1	1	0 thru 111	0000h – 1BFFh	14MB
1	1	1	0	0	0 thru 127	0000h - 1FFFh	16MB
1	1	1	0	1	0 thru 143	0000h - 23FFh	18MB
1	1	1	1	0	0 thru 159	0000h - 27FFh	20MB
1	1	1	1	1	ALL	0000h – 2FFFh	24MB

Note:

(1) If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

9.2 Configuration Register

9.2.1 One Time Program Lock Bit (OTP-L)

OTP-L is non-volatile.

The device provides an OTP area for the system to store critical data that cannot be changed once it's locked. The OTP area consists of 62 full pages. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from "1" to "0", and the OTP area cannot be erased.

Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

9.2.2 Enter OTP Access Mode Bit (OTP-E)

The OTP-E bit must be set to 1 in order to use the standard Program/Read commands to access the OTP area as well as to read the Unique ID / Parameter Page information. The default value after power up is 0.

9.2.3 ECC Enable Bit (ECC-E)

The device has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the spare area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be changed by the Device Reset command.

The power up default value of ECC-E bit is decided by DEFECC-E bit.

9.2.4 Output Driver Strength (DRV1-0)

Table 7 Output Driver Strength

DRV1	DRV0	Output Driver Strength
0	0	100% (default)
0	1	75%
1	0	50%
1	1	25%

9.2.5 Quad Enable Bit (QE)

The Quad Enable (QE) bit is a volatile bit, while it is "0" (factory default), it performs non-Quad and WP#, HOLD# are enabled. While QE is "1", it performs Quad I/O mode and WP#, HOLD# are disabled. In

another word, if the system goes into four I/O mode (QE=1), the WP# and HOLD# function will be disabled. Upon power cycle, the QE bit will go into the factory default setting "0".

9.2.6 Buffer Read Mode Bit (BUF)

The device provides two different modes for read operations, Buffer Read Mode (BUF=1) and Sequential/Continuous Read Mode (BUF=0). Prior to any Read operation, a Page Data Read command is needed to initiate the data transfer from a specified page in the memory array to the Data Buffer. By default, after power up, the data in page 0 will be automatically loaded into the Data Buffer and the device is ready to accept any read commands.

The Buffer Read Mode (BUF=1) requires a Column Address to start outputting the existing data inside the Data Buffer.

The Sequential/Continuous Read Mode (BUF=0) doesn't require the starting Column Address. The device will always start output the data from the first column (Byte 0) of the Data buffer, and once the end of the data buffer (set by CONT) is reached, the data output will continue through the next memory page. With Sequential Read Mode, it is possible to read out the entire memory array using a single read command. Please refer to respective command descriptions for the dummy cycle requirements for each read commands under different read modes.

In Sequential Read Mode, for each read instruction: 03h, 0Bh, 3Bh and 6Bh, the CA [15:0] address input becomes dummy input. The read must start from the beginning of the page.

The power up default value of BUF bit is decided by DEFBUF bit.

Please note:

1. Sequential/Continuous Read Mode does NOT support DTR mode
2. When read from cache command finish, the device may be busy for a period of time (tRDSTOP) to complete internal operation，the 0Fh (GET FEATURE) may be used to poll the status.

9.2.7 Continuous Read Bit (CONT)

Continuous Read Bit control the data output length for sequential read.

Table 8 Read Mode Definition

BUF	CONT	ECC-E	Max Data Output Length	ECC Status	Read Mode
1	Don't Care	0	2112	N/A	Buffer Read
1	Don't Care	1	2112	Page Based	Buffer Read
0	0	0	2112	N/A	Sequential without internal ECC
0	0	1	2112	Operation based	Sequential with internal ECC
0	1	0	2048	N/A	Continuous Read without internal ECC
0	1	1	2048	Operation based	Continuous Read with internal ECC

The power up default value of CONT bit is decided by DEFCONT bit.

9.2.8 Default value of ECC-E bit (DEFECC-E)

DEFECC-E bit is non-volatile.

DEFECC-E bit define power up default value of ECC-E. If DEFECC-E is 1 after power up, then power up default value of ECC-E bit is 1, else 0.

DEFECC-E bit shipment default value is 1, it can be written to 0 once. The sequence is as follows:
1. Issue Set Feature command (1Fh) to set BP3-0=1111
2. Issue Set Feature command (1Fh) to set OTP-E=0, ECC-E=1
3. Issue Set Feature command (1Fh) to set CONT=BUF=0
4. Issue Set Feature command (1Fh) to set DEFECC-E=0
5. Issue WREN command (06h) to set WEL bit
6. Issue Program Execute command (10h), page address is FF_FFh
7. Issue Get Feature command (0Fh) to read the OIP bit to check if program finish
8. Issue Get Feature command (0Fh) to read out ECC-E, check ECC-E=0 if success.

After the operation, ECC_E bit power up default value is **permanently** changed to 0.
The user can still change the value of ECC_E bit by Set Feature command. The value of DEFECC-E is permanently set to 0 and can NOT be set to 1 again.

9.2.9 Default value of CONT bit (DEFCONT)

DEFCONT bit is non-volatile.

DEFCONT bit define power up default value of CONT. If DEFCONT is 1 after power up, then power up default value of CONT bit is 1, else 0.

DEFCONT bit shipment default value is 1, it can be written to 0 once. The sequence is as follows:
1. Issue Set Feature command (1Fh) to set BP3-0=1111
2. Issue Set Feature command (1Fh) to set OTP-E=0, ECC-E=0
3. Issue Set Feature command (1Fh) to set CONT=1，BUF=0
4. Issue Set Feature command (1Fh) to set DEFCONT=0
5. Issue WREN command (06h) to set WEL bit
6. Issue Program Execute command (10h), page address is FF_FFh
7. Issue Get Feature command (0Fh) to read the OIP bit to check if program finish
8. Issue Get Feature command (0Fh) to read out CONT, check CONT=0 if success

After the operation, CONT bit power up default value is **permanently** changed to 0.
The user can still change the value of CONT bit by Set Feature command. The value of DEFCONT is permanently set to 0 and can NOT be set to 1 again.

9.2.10 Default value of BUF bit (DEFBUF)

DEFBUF bit is non-volatile.

DEFBUF bit define power up default value of BUF. If DEFBUF is 1 after power up, then power up default value of BUF bit is 1, else 0.

DEFBUF bit shipment default value is 1, it can be written to 0 once. The sequence is as follows:

1. Issue Set Feature command (1Fh) to set BP3-0=1111
2. Issue Set Feature command (1Fh) to set OTP-E=0, ECC-E=0
3. Issue Set Feature command (1Fh) to set CONT=0，BUF=1
4. Issue Set Feature command (1Fh) to set DEFBUF=0
5. Issue WREN command (06h) to set WEL bit
6. Issue Program Execute command (10h), page address is FF_FFh
7. Issue Get Feature command (0Fh) to read the OIP bit to check if program finish
8. Issue Get Feature command (0Fh) to read out BUF, check BUF=0 if success.

After the operation, BUF bit power up default value is **permanently** changed to 0.
The user can still change the value of BUF bit by Set Feature command. The value of DEFBUF is permanently set to 0 and can NOT be set to 1 again.

9.3 Status Register

9.3.1 ECC Status Bit (ECCS1-0)

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECCS1, ECCS0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits value are don't care if ECC-E=0. These bits will be cleared to 0 after a RESET command.

The ECCS1-0 value reflects the ECC status of the content of the page 0 of block 0 after a power-on reset.

Table 9 ECC Bits Status

ECCS1	ECCS0	Description
0	0	No bit errors were detected during the previous read operation
0	1	1-bit error was detected in one or more sector and was corrected
1	X	More than 1-bit error was detected in one or more sector and cannot be corrected

9.3.2 Program/Erase Failure (P-FAIL, E-FAIL)

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. P-FAIL bit will also be set when the Program command is issued to a protected block or locked OTP area, and E-FAIL bit will also be set when the Erase command is issued to a protected block. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device Reset command.

9.3.3 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit. The WEL bit is set to 1 after executing a Write Enable Instruction. The WEL bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read, and Program Execute for OTP pages.

9.3.4 Operation in Progress (OIP)

OIP is a read only bit that is set to a 1 state when the device is powering up or executing a Page Read, Program Execute, Block Erase and OTP Locking. During this time the device will ignore further instructions except for the Get Feature or Soft Reset instructions. When the program, erase or page read instruction has completed, the OIP bit will be cleared to a 0 state indicating the device is ready for further instructions.

9.3.5 Look-Up Table Full (LUT-F)

To facilitate the NAND flash memory bad block management, the device is equipped with an internal Bad

Block Management Look-Up-Table (BBM LUT). Up to 8 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 8 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 8 links are used, LUT-F will become 1, and no more memory block links may be established.

9.4 Sector ECC Status Register

A sector is composed by a 512 Byte main area and a 16 Byte spare area, so a page has four sectors.

The Sector ECC Status Register indicates the number of errors in each sector as identified from an ECC check during a read operation.

Table 10 2K Byte Page Assignment

1st Main	2nd Main	3rd Main	4th Main	1st Spare	2nd Spare	3rd Spare	4th Spare
512B	512B	512B	512B	16B	16B	16B	16B

Table 11 Definition of 528Btye Sector

Sector	Column Address (Byte)	
	Main Field	Spare Field
1st Sector	000h ~ 1FFh	800h ~ 80Fh
2nd Sector	200h ~ 3FFh	810h ~ 81Fh
3rd Sector	400h ~ 5FFh	820h ~ 82Fh
4th Sector	600h ~ 7FFh	830h ~ 83Fh

Table 12 ECC Status Register0-3

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Sector Information				Sector ECC Status			

Table 13 Sector Information

Bit 7 ~ Bit 4	Sector Information
0000	1st Sector (Main and Spare area)
0001	2nd Sector (Main and Spare area)
0010	3rd Sector (Main and Spare area)
0011	4th Sector (Main and Spare area)
Other	Reserved

Table 14 Sector ECC Status

Bit 3 ~ Bit 0	Sector ECC Status
0000	No bit error was detected during the previous read operation
0001	One bit error was detected in the sector and was corrected
001x	More than one bit errors were detected in the sector and cannot be corrected
Others	Reserved

10 Commands

10.1 Command Set

Table 15 Command Set

Commands	Byte1	Byte2	Byte3	Byte4	Byte5	ByteN
Soft RESET	**FFh**					
Enable Power on Reset	**66h**					
Power on Reset	**99h**					
Read JEDEC ID	**9Fh**	Dummy	MID	DID	DID	
Get Feature	**0Fh**	SR Addr	S7-0	S7-0	S7-0	S7-0
Set Feature	**1Fh**	SR Addr	S7-0			
Write Enable	**06h**					
Write Disable	**04h**					
Add BBM LUT	**A1h**	LBA	LBA	PBA	PBA	
Read BBM LUT`	**A5h**	Dummy	LBA0	LBA0	PBA0	PBA0
ECC Failure Page Address	**A9h**	Dummy	PA15-8(L)	PA7-0(L)	PA15-8(F)	PA7-0(F)
Block Erase	**D8h**	**PA23-16**	**PA15-8**	**PA7-0**		
Program Data Load	**02h**	**CA15-8**	**CA7-0**	D7-D0	Next Byte	…
Random Program Data Load	**84h**	**CA15-8**	**CA7-0**	D7-D0	Next Byte	…
Quad Program Data Load	**32h**	**CA15-8**	**CA7-0**	D7-D0 / 4	Next Byte	…
Random Quad Program Data Load	**34h**	**CA15-8**	**CA7-0**	D7-D0 / 4	Next Byte	…
Program Execute	**10h**	**PA23-16**	**PA15-8**	**PA7-0**		
Page Read (to cache)	**13h**	**PA23-16**	**PA15-8**	**PA7-0**		
Read From Cache	**03h or 0Bh**	**CA15-8**	**CA7-0**	Dummy	D7-D0	Next Byte
Read From Cache x 2	**3Bh**	**CA15-8**	**CA7-0**	Dummy	D7-D0 / 2	Next Byte
Read From Cache x 4	**6Bh**	**CA15-8**	**CA7-0**	Dummy	D7-D0 / 4	Next Byte
DTR Read	**0Dh**	**CA15-0**	Dummy	D7-D0 / 2	Next Byte	…
DTR Read Dual Output	**3Dh**	**CA15-0**	Dummy	D7-D0 / 4	Next Byte	…
DTR Read Quad Output	**6Dh**	**CA15-0**	Dummy	D7-D0 / 8	Next Byte	…

Note:

(1) Output designates data output from the device.

(2) Column Address (CA) only requires CA [11:0], CA [15:12] are considered as dummy bits.

(3) Page Address (PA) only requires PA [14:0], PA [23:15] are considered as dummy bits. PA [14:6] is the address for 128kB blocks (total 512 blocks), PA [5:0] is the address for 2kB pages (total 64 pages for each block).

(4) Dual SPI Data Output (D7-D0 / 2) format:
SIO0 = D6, D4, D2, D0…
SIO1 = D7, D5, D3, D1…

(5) Quad SPI Data Input / Output (D7-D0 / 4) format:
SIO0 = D4, D0 ……
SIO1 = D5, D1 ……
SIO2 = D6, D2 ……
SIO3 = D7, D3 ……

(6) All Quad Program/Read commands are disabled when QE bit is set to 0 in the Configuration Register.

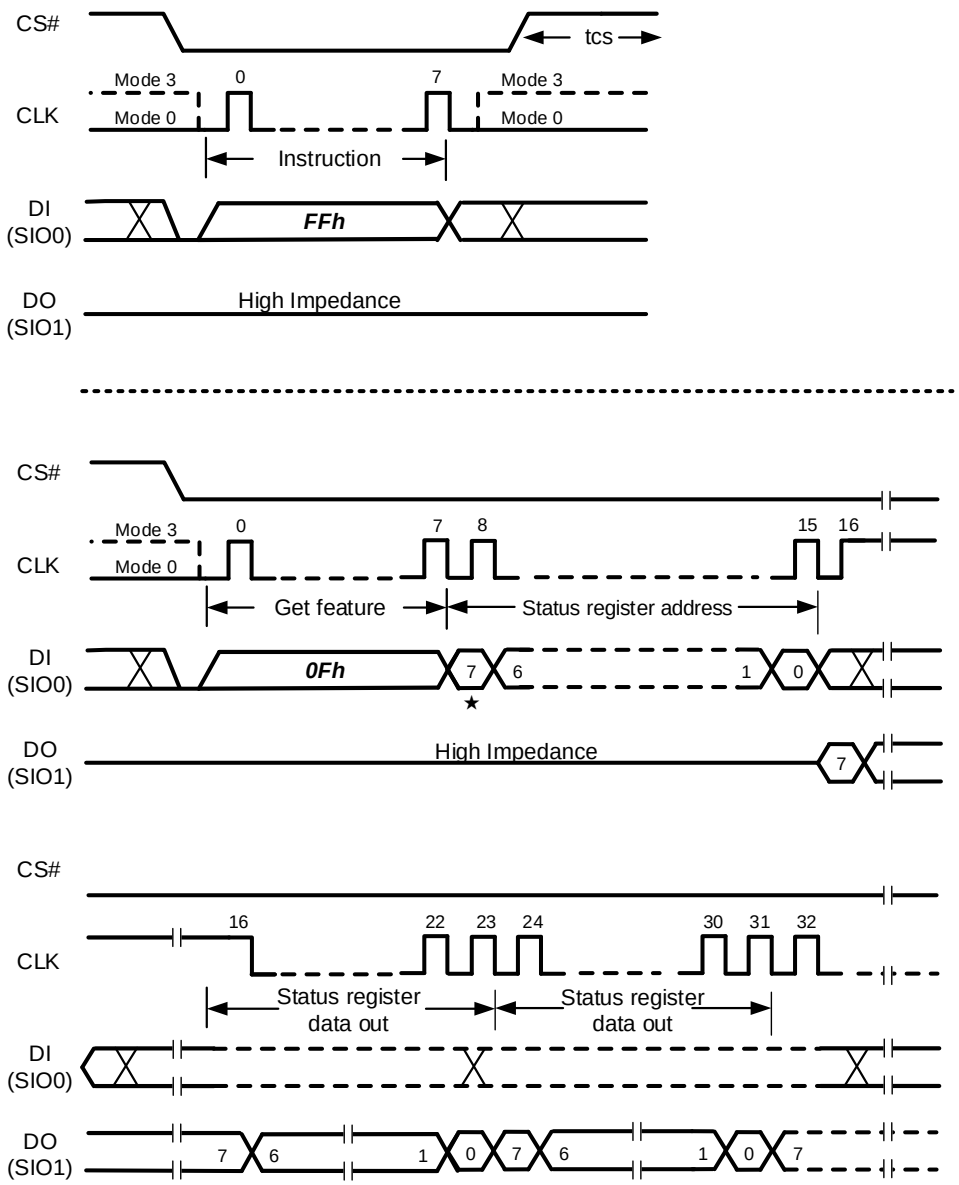
(7) For DTR read, command input is in STR mode, while address input and data output are in DTR mode with 8 dummy clocks.

10.2 Soft Reset (FFh)

Once the Reset command is accepted by the device, the device will take approximately t_{RST} to reset, depending on the current operation the device is performing, t_{RST} can be 5us~200us. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command is accepted by the device. It is recommended to check the OIP bit in Status Register before issuing the Reset command.

Figure 9 Soft Reset Sequence



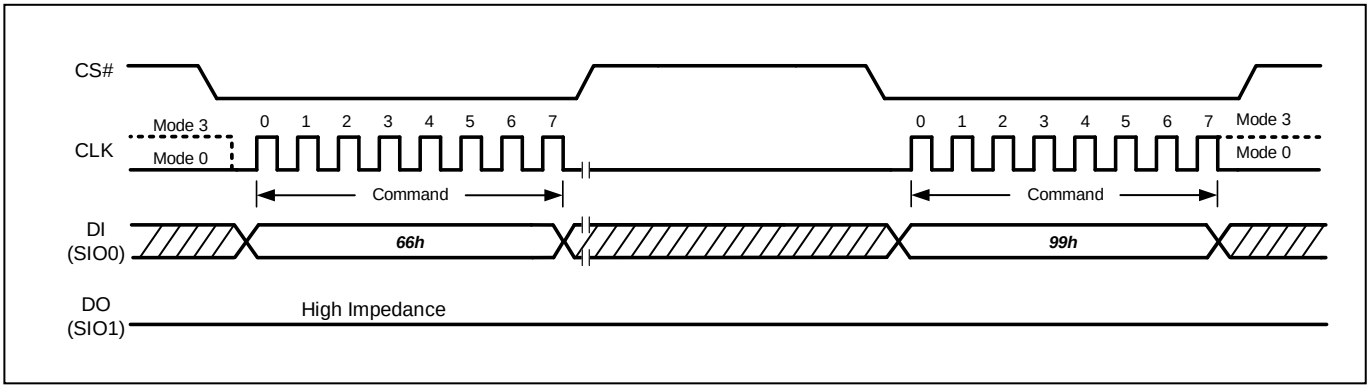
10.3 Enable Power on Reset (66h) and Power on Reset (99h)

If the Power on Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current feature settings.

The “Enable Reset (66h)” and the “Reset (99h)” commands can be issued in SPI mode. The “Reset (99h)” command sequence as follow: CS# goes low -> Sending Enable Reset command ->CS# goes high ->CS# goes low.->Sending Reset command ->CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tPUW to reset. During this period, no command will be accepted. It is recommended to check the OIP bit in Status Register before issuing any other command sequence. The contents of the memory location being programmed or the block being

erased are no longer valid.

Figure 10 Reset Sequence Diagram



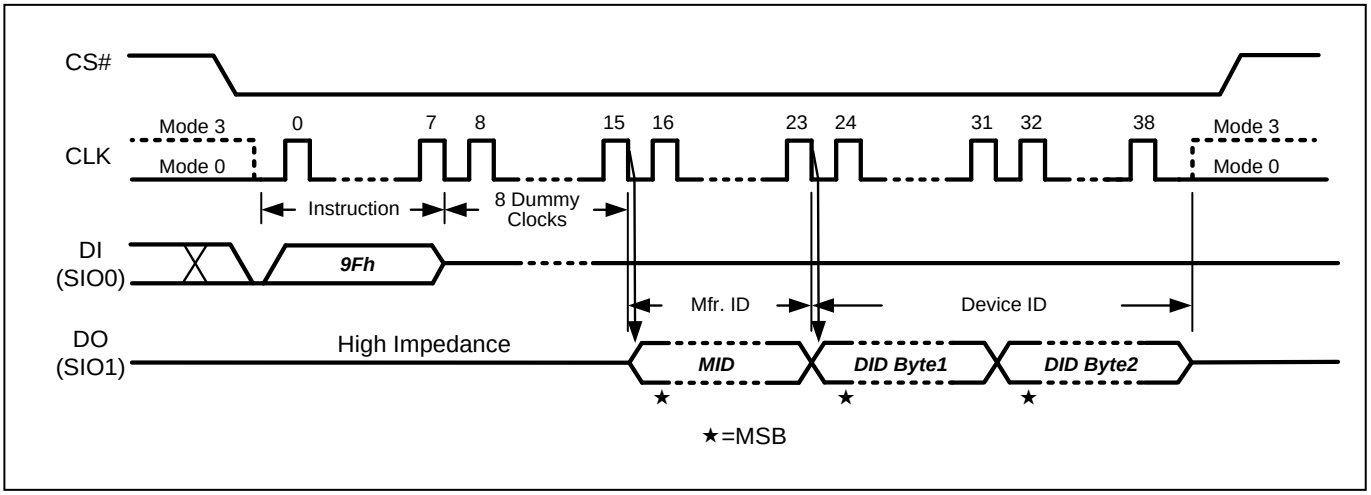
10.4 Read JEDEC ID (9Fh)

The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

Table 16 JEDEC ID

ID		Value
Manufacture ID		CDh
Device ID	Byte 1	F1h
	Byte 2	F1h

Figure 11 Read JEDEC ID



10.5 Feature Operations

10.5.1 Get Feature (0Fh) and Set Feature (1Fh)

The Get Feature (0Fh) and Set Feature (1Fh) commands are used to monitor the device status and alter the device behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific feature bits. The status register is mostly read, except WEL, which is a writable bit with the Write Enable (06h) and Write Disable (04h) command. When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified, once the device is set, it remains set, even if a RESET (FFH) command is issued. Refer to **Status Registers** for detail information.

Figure 12 Get Feature

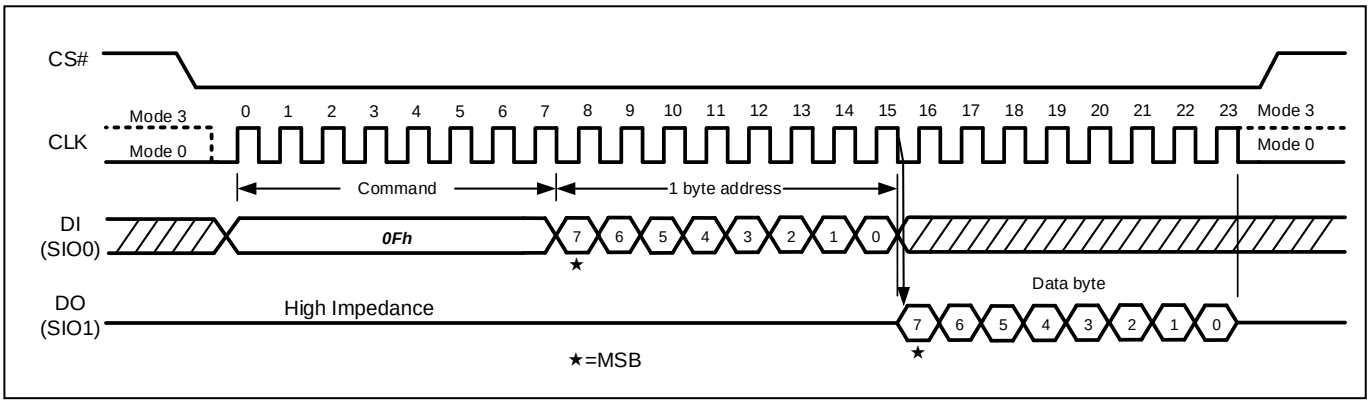
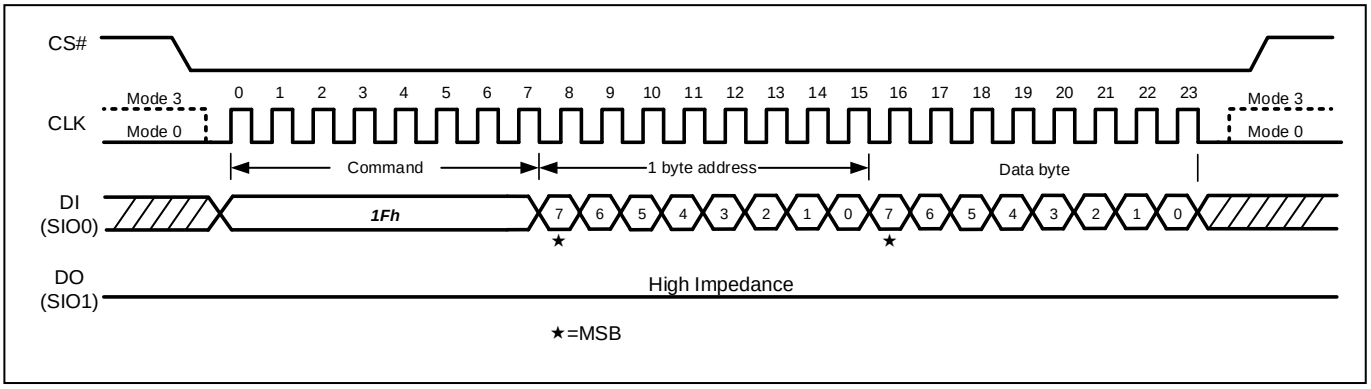


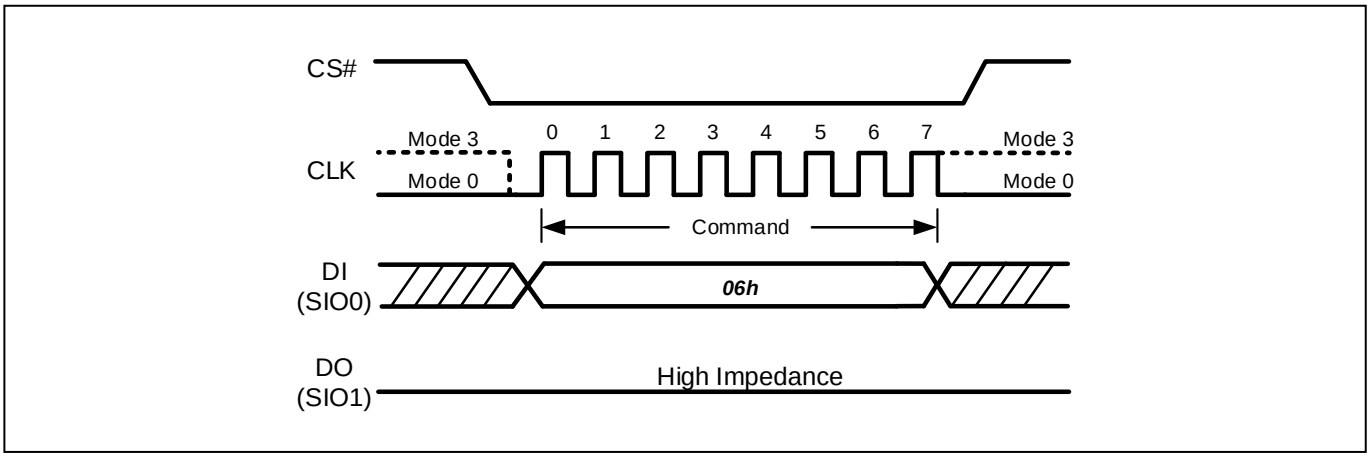
Figure 13 Set Feature



10.5.2 Write Enable (WREN, 06h)

The Write Enable (WREN, 06h) command is for setting Write Enable Latch (WEL) bit. The WEL bit must be set prior to every Page Program, Block Erase and OTP.

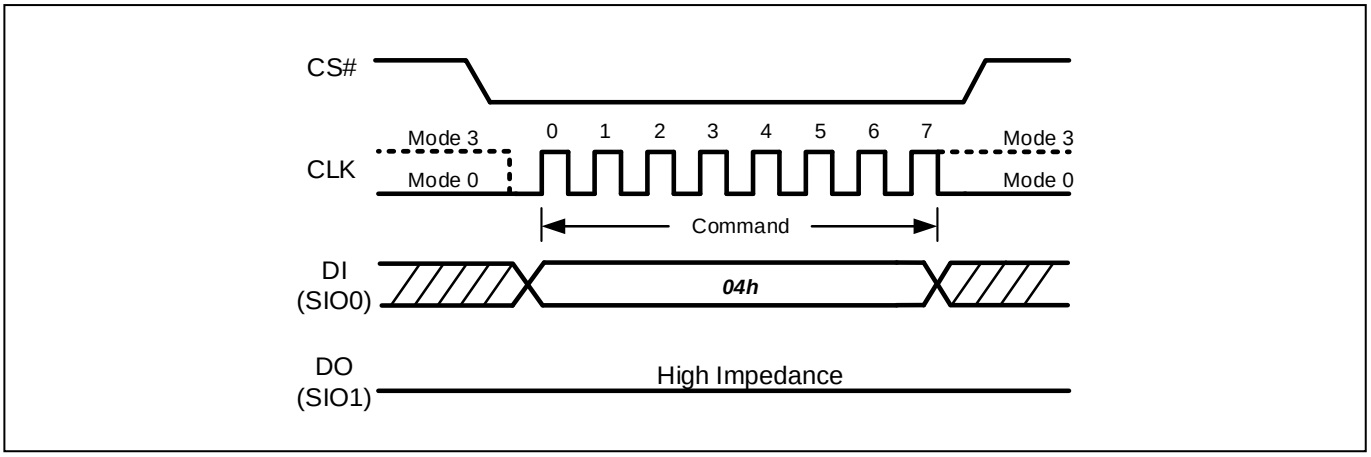
Figure 14 Write Enable Sequence



10.5.3 Write Disable (WRDI, 04h)

The Write Disable (WRDI, 04h) instruction is to reset Write Enable Latch (WEL) bit. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Program, Block Erase, and Reset commands.

Figure 15 Write Disable Sequence



10.6 Read Operations

The device supports Power-on Read function, after power up, the device will automatically load the data of the 1st page of 1st block from array to cache. The host micro-controller may directly read the 1st page of 1st block data from the cache buffer.

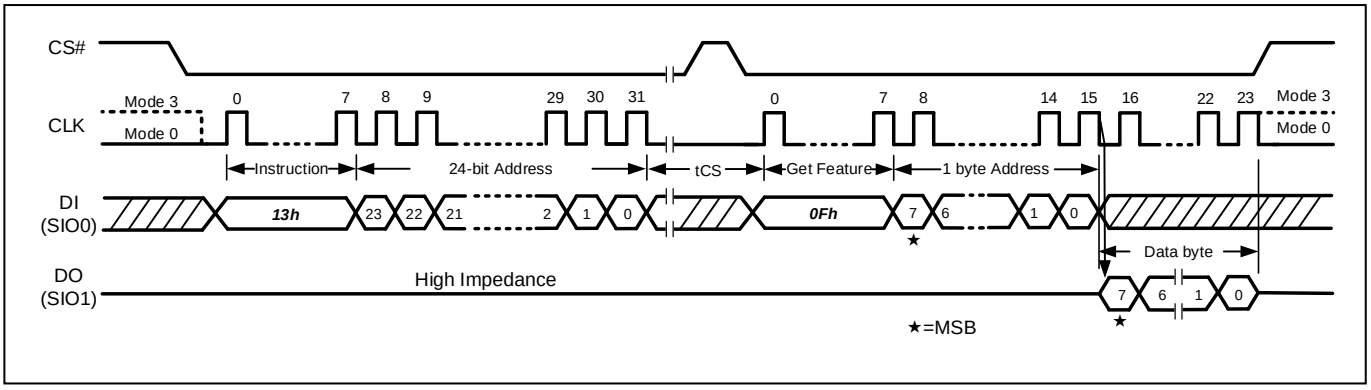
10.6.1 Page Read (13h)

The page read operation transfers data from array to cache by issuing the Page Read (13h) command followed by the 24-bit address (including the dummy/block/page address).

The device will have a period of time (tRD or tRD_{ECC}) being busy after the CS# goes high. The Get Feature command may be used to poll the operation status.

After read operation is completed, the Read from Cache (03h or 0Bh), Read from cache (x2) (3Bh), Read from cache (x4) (6Bh) may be issued to fetch the data.

Figure 16 Page Read Sequence



10.6.2 Read From Cache (03h or 0Bh)

The Read From Cache command allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page command.

Figure 17 Read From Cache (03h) Sequence

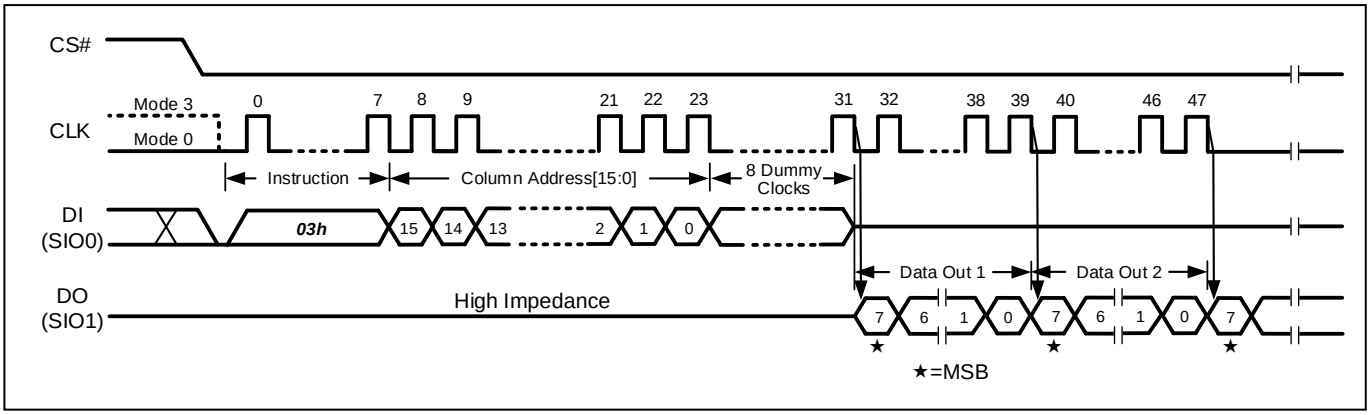
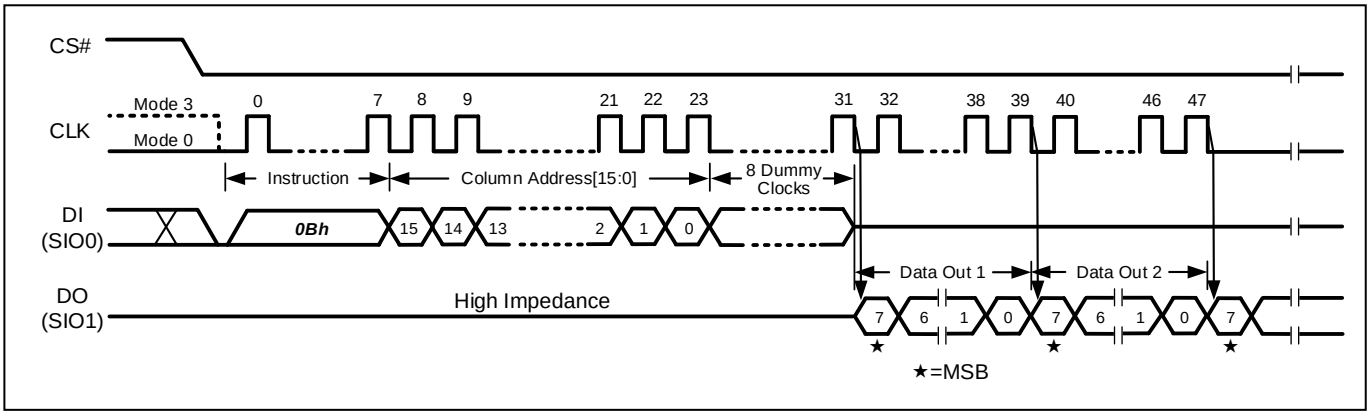


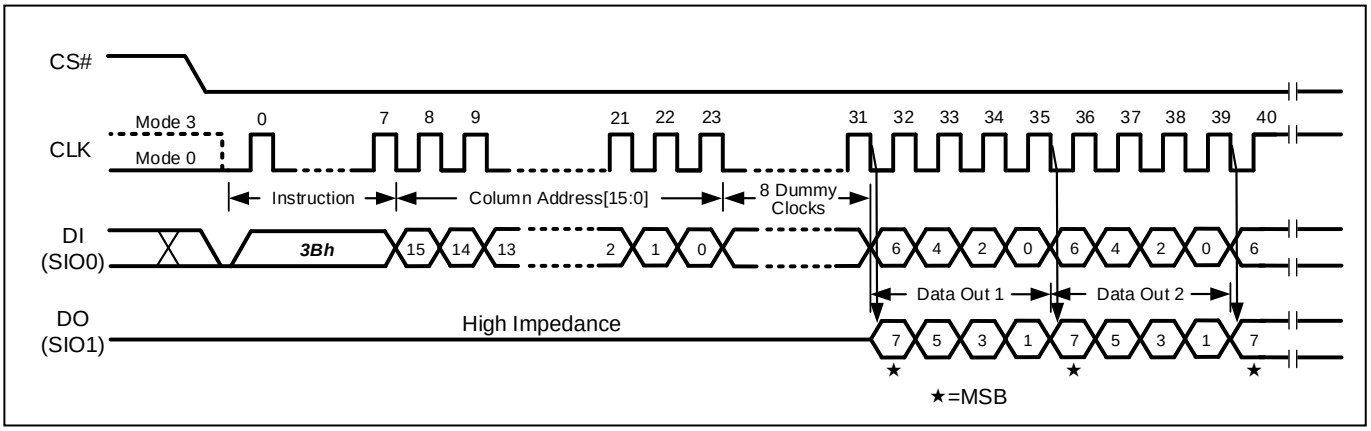
Figure 18 Read From Cache (0Bh) Sequence



10.6.3 Read From Cache x 2 (3Bh)

The Read From Cache x 2 command is similar to the Read From Cache command except that data is output on two pins: SIO0 and SIO1. This allows data to be transferred at twice the rate of standard SPI devices.

Figure 19 Read From Cache x2 (3Bh) Sequence

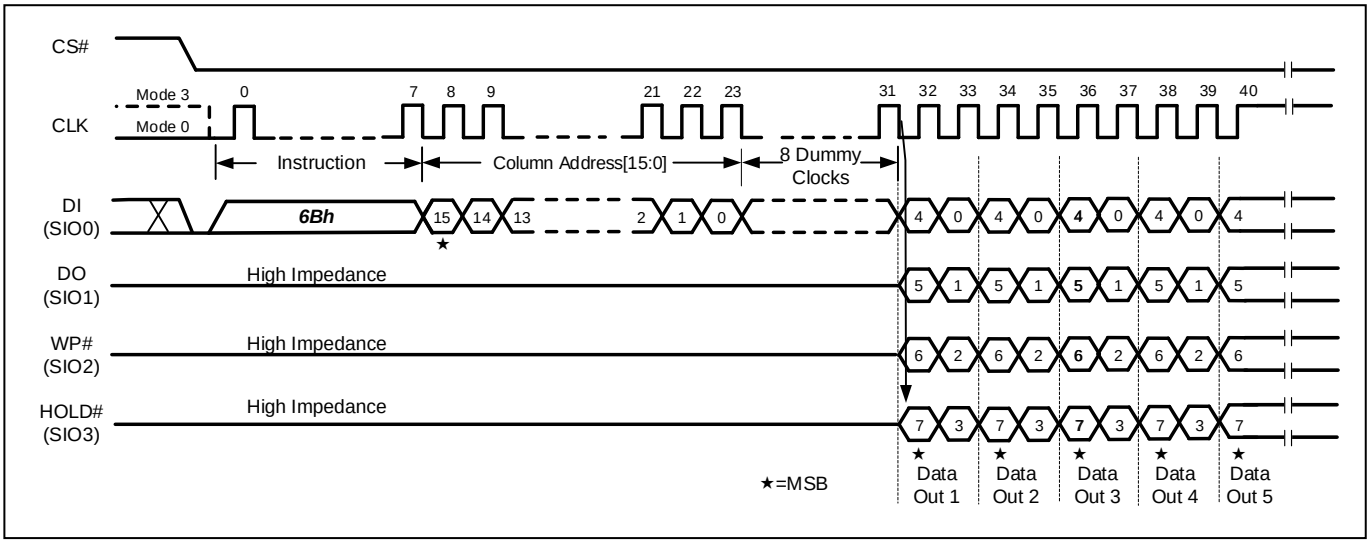


10.6.4 Read From Cache x 4 (6Bh)

The Read From Cache x 4 command is similar to the Read From Cache x 2 command except that data is output on four pins: SIO0, SIO1, SIO2 and SIO3. This allows data to be transferred at four times the rate of standard SPI devices.

When QE bit in the Status Register is set to a 0, this command is disabled.

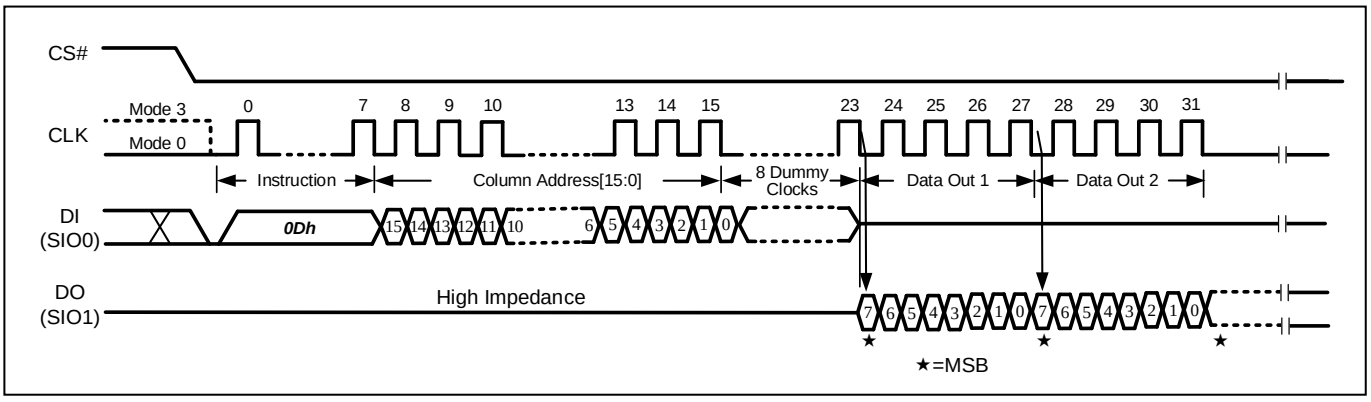
Figure 20 Read From Cache x4 (6Bh) Sequence



10.6.5 DTR Read (0Dh)

The DTR Read command allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page command. Address shift in and data shift out are valid at the both edge of CLK, which differs to the Read From Cache command.

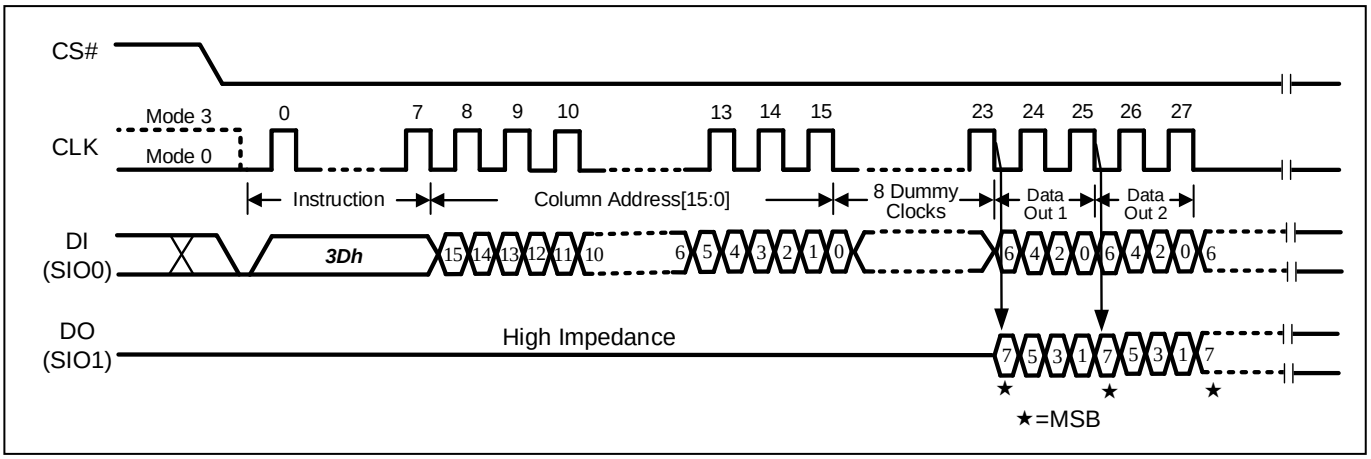
Figure 21 DTR Read (0Dh) Sequence



10.6.6 DTR Read Dual Output (3Dh)

The DTR Read Dual Output command is similar to the DTR Read command except that data is output on two pins: SIO0 and SIO1.

Figure 22 DTR Read Dual Output (3Dh) Sequence

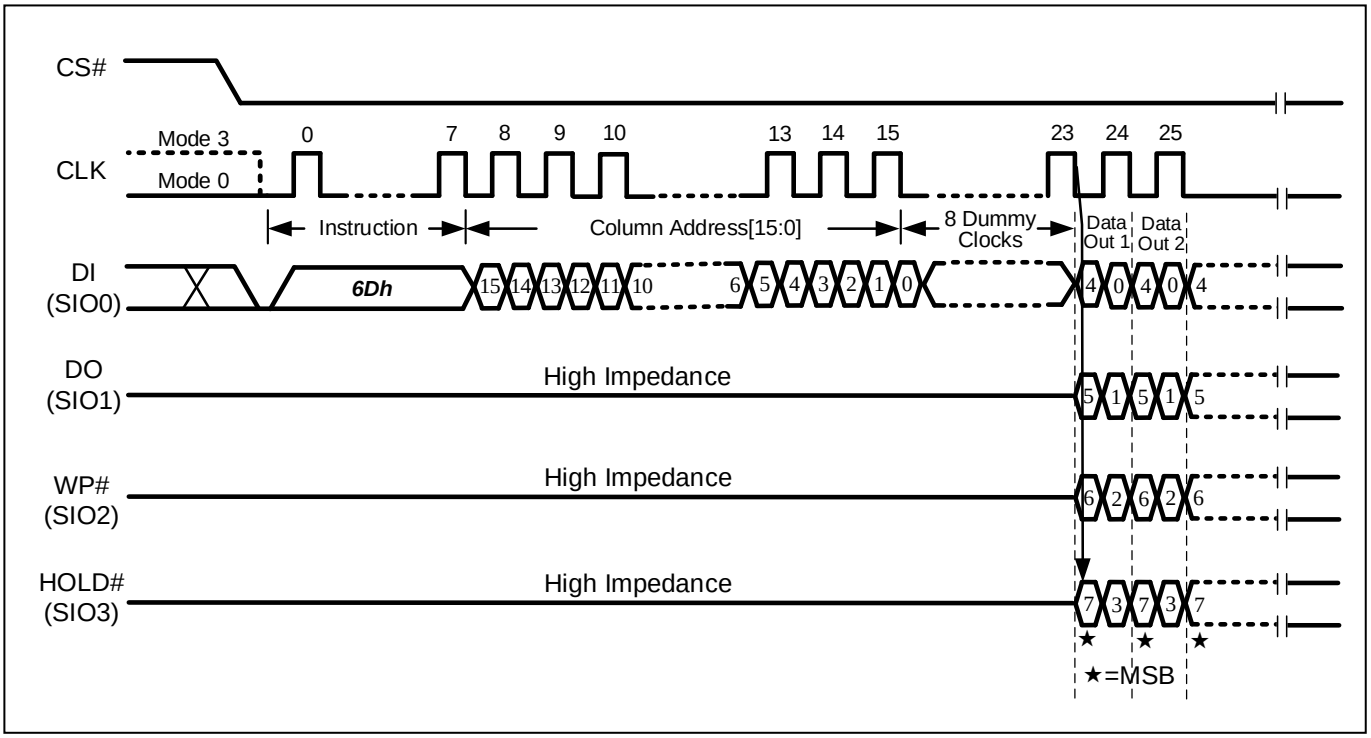


10.6.7 DTR Read Quad Output (6Dh)

The DTR Read Quad Output command is similar to the DTR Read Dual Output command except that data is output on four pins: SIO0, SIO1, SIO2 and SIO3.

When QE bit in the Status Register is set to a 0, this command is disabled.

Figure 23 DTR Read Quad Output (6Dh) Sequence



10.7 Program Operations

10.7.1 Page Program

The Page Program operation sequence programs 1 byte to whole page of data within a page. The page program sequence is as follows:

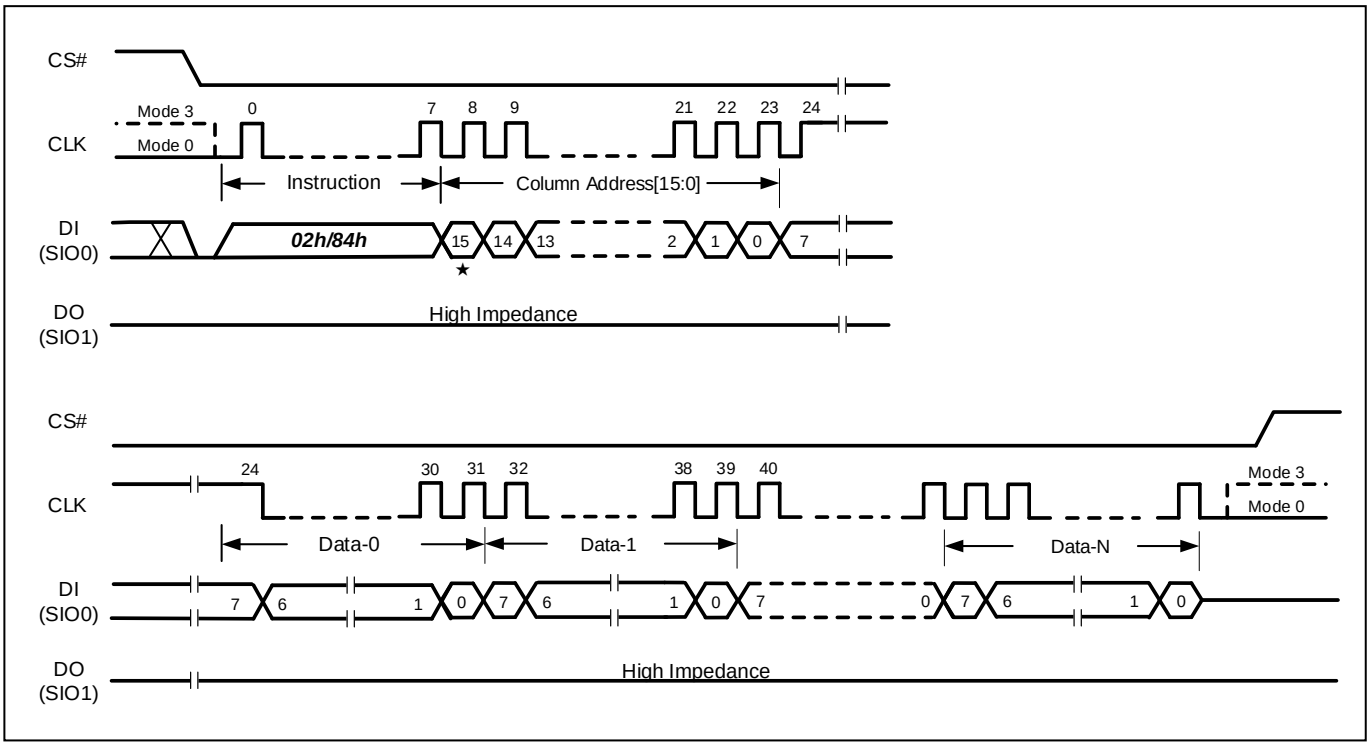
1. Issue Program Data Load (02h) / Program Data Load x4 (32h)
2. Issue Write Enable command (06h)
3. Issue Program Execute command (10h)
4. Issue Get Feature command (0Fh) to read the status

10.7.2 Program Data Load (02h) / Random Program Data Load (84h)

The Program Data Load or Random Program Data Load command is used to load the program data into the data buffer. The command is initiated by driving the CS# pin low then shifting the command code “02h” or “84h” followed by a 16-bit column address (only CA[11:0] is effective) and at least one byte of data into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device.

Program Data Load command will reset the unused data bytes in the Data Buffer to FFh value, while Random Program Data Load command will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

Figure 24 (Random) Program Data Load Sequence



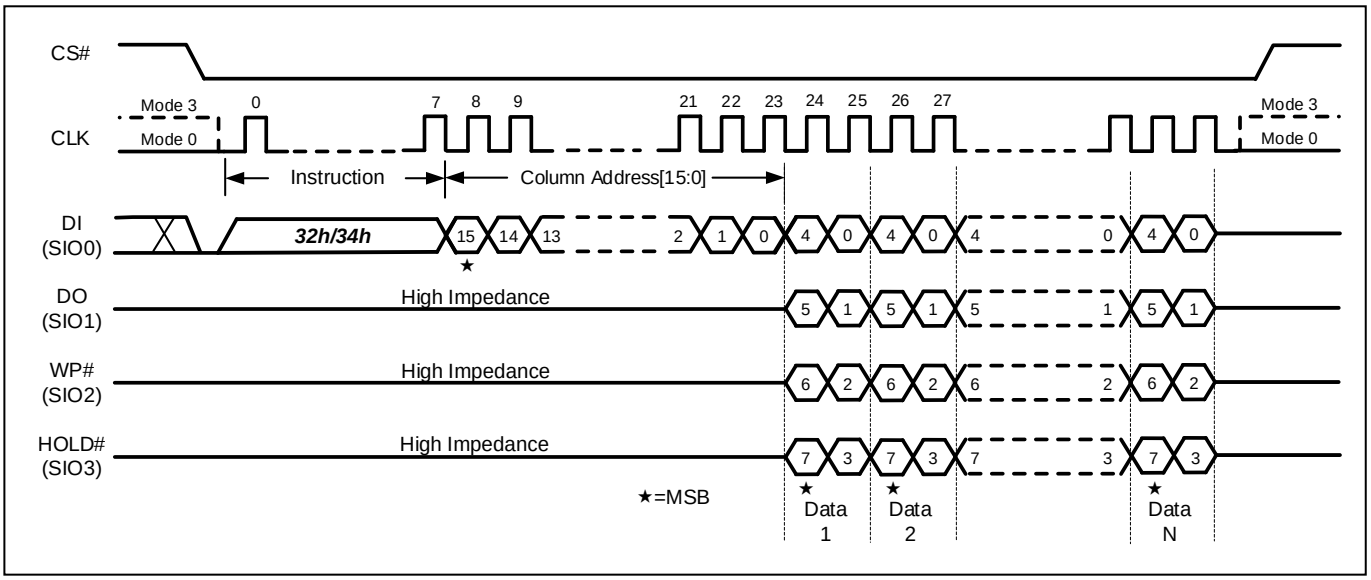
10.7.3 Program Data Load x 4 (32h) / Random Program Data Load x 4 (34h)

The Program Data Load x 4 and Random Program Data Load x 4 commands are similar to the Program Load Data and Random Program Load Data, the only difference is that “x4” commands will input the data bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer.

Program Data Load x 4 command will reset the unused data bytes in the Data Buffer to FFh value, while Random Program Data Load x 4 instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

When QE bit in the Status Register is set to 0, all Quad SPI instructions are disabled.

Figure 25 (Random) Program Data Load x4 Sequence



10.7.4 Program Execute (10h)

The Program Execute command will program the Data Buffer content into the physical memory page that is specified in the command. Prior to performing the Program Execute operation, a Write Enable (06h) command must be issued to set the WEL bit.

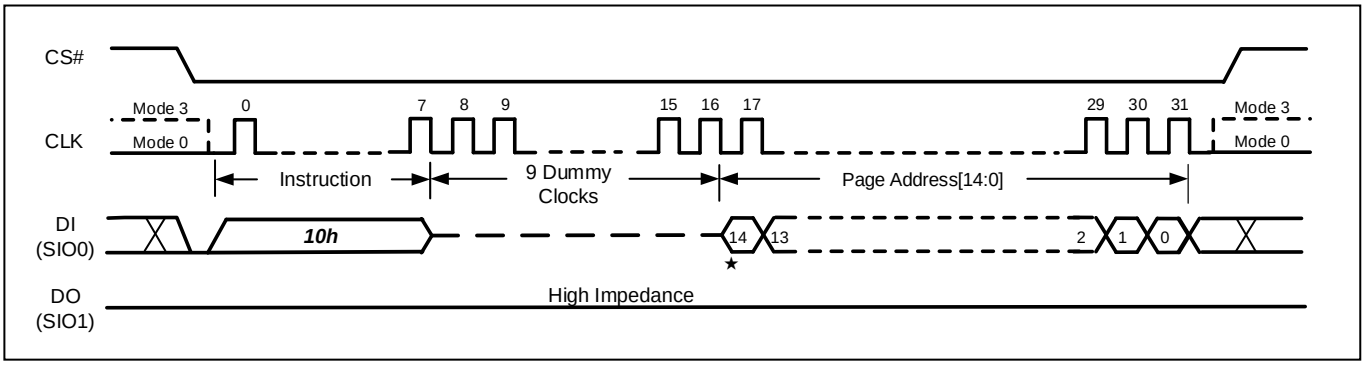
The Program Execute command is initiated by driving the CS# pin low then shifting the instruction code “10h” followed by 9-bit dummy clocks and 15-bit Page Address into the DI pin.

After CS# is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for time duration of tPROG or $tPROG_{ECC}$. While the Program Execute cycle is in progress, the Get Feature command (0Fh) may be used for checking the status of the OIP bit. The OIP bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute command will not be executed if the addressed page is protected by the Block Protect (TB, BP3, BP2, BP1, and BP0) bits. Only 1 partial

page program time is allowed on every single page.

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.

Figure 26 Program Execute Sequence



10.7.5 Internal Data Move

The Internal Data Move command sequence programs or replaces data in a page with existing data. The sequence is as follows:

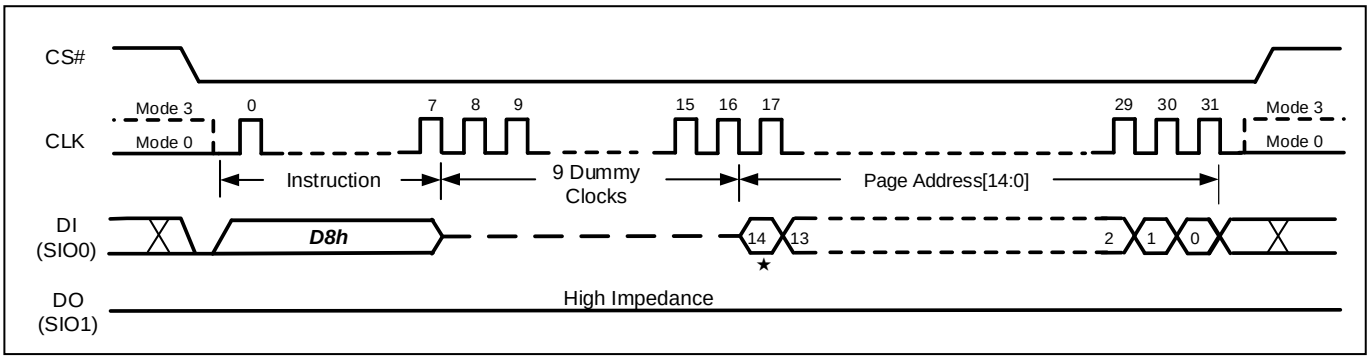
1. Issue Page Read command (13h)
2. Random Program Data Load (Optional)
3. Issue Write Enable command (06h)
4. Issue Program Execute command (10h)
5. Issue Get Feature command (0Fh) to read the status

Prior to performing an internal data move operation, the target page content must be read out into the cache register by issuing a Page Read (13h) command. One or more Random Program Data Load (84h/34h) command can be issued, if user wants to update bytes of data in the page. After the data is loaded, the Write Enable command (06h) and the Program Execute (10h) command can be issued to start the program operation.

10.8 Block Erase Operations

The Block Erase instruction sets all memory within a specified block to the erased state of all 1s (FFh). A Write Enable command must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low and shifting the command code “D8h” followed by 9-bit dummy clocks and 15-bit page address.

Figure 27 Block Erase Sequence



10.9 UID / Parameter / OTP Pages

In addition to the main memory array, the device has one Unique ID Page, one Parameter Page, and sixty-two OTP Pages.

Table 17 UID / Parameter / OTP Pages

Page Address PA[15:0]	Page Name	Descriptions	Data Length
00_00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
00_01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
00_02h	OTP Page [0]	Program Only, OTP lockable	Full Page
00_03h	OTP Page [1]	Program Only, OTP lockable	Full Page
…	…	…	…
00_3Fh	OTP Page [61]	Program Only, OTP lockable	Full Page

Unique ID Page: To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies (each copy has 32 bytes) of the UID and the corresponding complement are stored. On each 32-byte, the first 16-byte and following 16-byte are complementary. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid.

Parameter Page: Contains at least three identical copies of the 256-Byte Parameter Data.

To access these additional data pages, the OTP-E bit in Configuration Register must be set to “1” first. Then read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it’s not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

10.9.1 Read UID / Parameter / OTP Pages

The Read UID / Parameter / OTP pages sequence is as follows:

1. Issue Set Feature command (1Fh) to set OTP-E=1.
2. Issue Page Read command (13h) with address shown in the table above.
3. Issue Get Feature command (0Fh) to read the status.
4. Issue Read from cache command (03h/0Bh/3Bh/6Bh) to read data.

Note:

(1) For OTP pages, Internal ECC can be enabled for the OTP page read operations to ensure the data integrity.

(2) When reading UID / Parameter page, Internal ECC is internally disabled by the chip.

10.9.2 Program OTP Pages and OTP Lock Operation

OTP pages provide the additional space (2K-Byte x 62) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state

set in the factory, and can only be programmed (change data from “1” to “0”) until being locked by OTP-L bit in the Configuration Register.

The Program OTP Pages sequence is as follows:
1. Issue Set Feature command (1Fh) to set OTP-E=1
2. Issue WREN command (06h) to set WEL bit
3. Issue Program Data Load and Program Execute command
4. Issue Get Feature command (0Fh) to read the status.

When ECC is enabled, ECC calculation will be performed during Program Execute.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible.

The OTP Lock sequence is as follows:
1. Issue Set Feature command (1Fh) to set OTP-E=1 and OTP-L=1
2. Issue WREN command (06h) to set WEL bit
3. Issue Program Execute command (10h), page address is “don’t care”
4. Issue Get Feature command (0Fh) to read the status.
5. Issue Set Feature command (1Fh) to set OTP-E=0, return to the main memory array operation.

10.9.3 Parameter Page Data Definition

Table 18 Parameter Definition

Byte Number	Descriptions	Values
0~3	Parameter Page Signature, "ONFI" ASCII characters	4Fh 4Eh 46h 49h
4~5	Revision Number	00h 00h
6~31	Reserved (0)	all 00h
32~43	Device manufacturer, 12 ASCII characters	46h 4Fh 52h 45h 53h 45h 45h 20h 20h 20h 20h 20h
44-63	Device Model, 20 ASCII characters	46h 33h 35h 53h 51h 41h 31h 39h 32h 4Dh 20h 20h 20h 20h 20h 20h 20h 20h 20h 20h
64	JEDEC MID	CDh
65-66	Date Code	00h 00h
67-79	Reserved (0)	all 00h
80-83	Number of Data Bytes per Page	00h 08h 00h 00h
84-85	Number of Spare Bytes per Page	40h 00h
86-89	Number of Data Bytes per Partial Page	00h 02h 00h 00h
90-91	Number of Spare Bytes per Partial Page	10h 00h
92-95	Number of Pages per Block	40h 00h 00h 00h

Byte Number	Descriptions	Values
96-99	Number of Block per Logic Unit	A0h 00h 00h 00h
100	Number of Logic Units	01h
101	Reserved (0)	00h
102	Number of Bits per Cell	01h
103-104	Bad Blocks Maximum per Logic Unit	04h 00h
105-106	Block Endurance	01h 05h
107	Guaranteed Valid Blocks at Beginning of Target	01h
108-109	Block Endurance for Guaranteed Valid Blocks	01h 03h
110	Number of Programs per Page	04h
111	Partial Programming Attributes b5-b7 reserved (0) b4 1 = partial page layout is partial page data followed by partial page spare b1-b3 reserved (0) b0 1 = partial page programming has constraints	00h
112	Number of ECC Bits Correct ability	01h
113-127	Reserved (0)	all 00h
128	I/O Pin Capacitance, Maximum	06h
129-132	Reserved (0)	all 00h
133-134	t_{PROG} Maximum Page Program Time (us)	D0h 02h
135-136	t_{ERS} Maximum Block Erase Time (us)	10h 27h
137-138	t_{RD} Maximum Page read Time (us)	3Ch 00h
139-163	Reserved (0)	all 00h
164-165	Vendor Specific Revision Number	00h 00h
166-253	Vendor Specific	all 00h
254-255	Integrity CRC	
256-511	Value of Bytes 0-255	
512-767	Value of Bytes 0-255	
768+	Additional Redundant Parameter Pages	

Note:

(1) The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details. The CRC shall be calculated using the following 16-bit generator polynomial: G(X) = X16 + X15 +X2 + 1

10.10 Bad Block Management

10.10.1 Add BBM LUT (A1h)

Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of “Bad Blocks” found in the factory testing. Up to 2% of the memory blocks can be marked as “Bad Blocks” upon shipment, which is a maximum of 4 blocks for the device. In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page.

The device offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The Add BBM LUT command is initiated by shifting the instruction code “A1h” into the DI pin and followed by the 16-bits “Logical Block Address” and 16-bits “Physical Block Address”. The logical block address is the address for the “bad” block that will be replaced by the “good” block indicated by the physical block address.

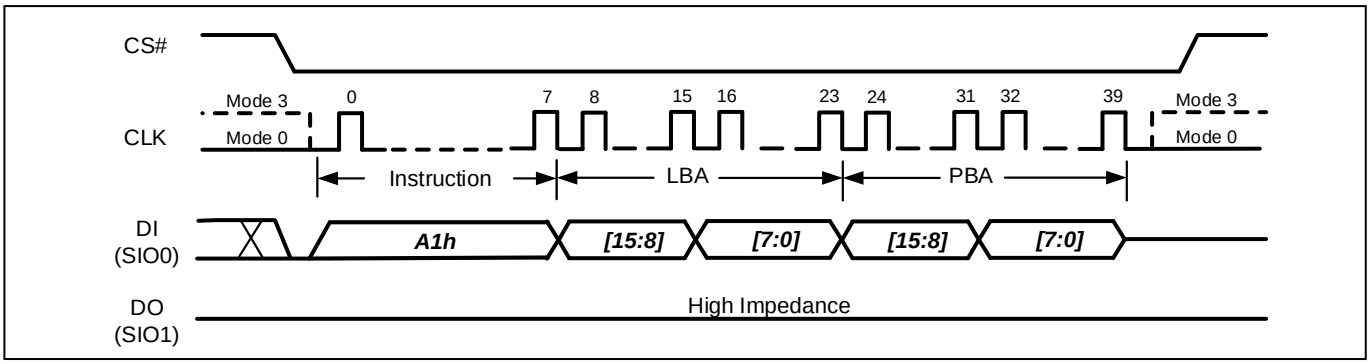
Prior to performing the Add BBM LUT operation, a Write Enable (06h) command must be issued to set the WEL bit. The Add BBM LUT command is initiated by driving the CS# pin low and shifting the instruction code “A1h” followed by 16-bits LBA (LBA[7:0] is Bad Block address, LBA[15:8] is don’t care) and the 16-bits PBA (PBA[7:0] is Good Block address, PBA[15:8] is don’t care). After CS# is driven high to complete the command cycle, the self-timed Add BBM LUT instruction will commence for a time duration of tPROG. While the Add BBM LUT cycle is in progress, the Get Feature command (0Fh) may still be used for checking the status of the OIP bit. The OIP bit is a 1 during the Add BBM LUT cycle and becomes a 0 when the cycle is finished, and the device is ready to accept other instructions again. After the Add BBM LUT cycle has finished, the WEL bit is cleared to 0.

Once an Add BBM LUT command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 8 links can be established in the non-volatile LUT. If all 8 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Add BBM LUT command, the LUT-F bit value can be checked or a “Read BBM LUT” command can be issued to confirm if spare links are still available in the LUT.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

To guarantee a continuous read operation on the first 128 blocks, the manufacturer may have used some of the BBM LUT entrees. It is advisable for the user to scan all blocks and keep a table of all manufacturer bad blocks prior to first erase/program operation.

Figure 28 Add BBM LUT Sequence



10.10.2 Read BBM LUT (A5h)

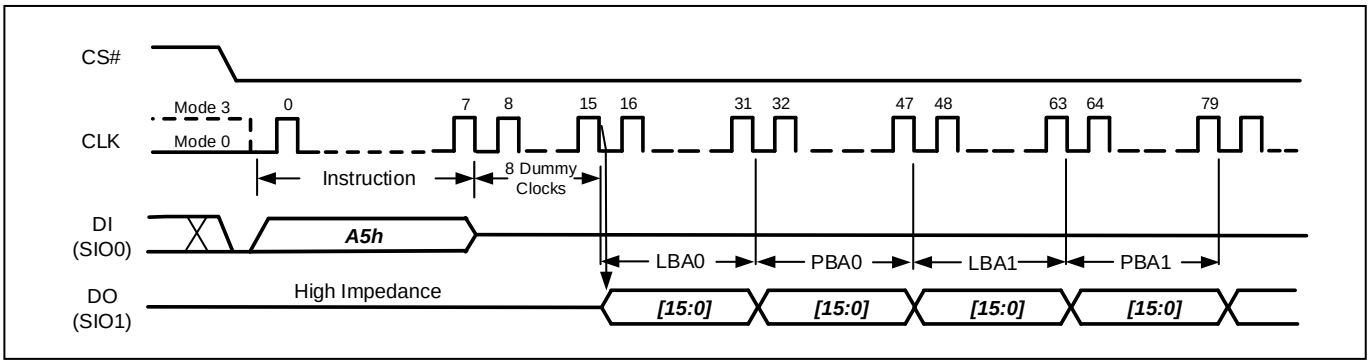
The internal Look Up Table (LUT) consists of 8 Logical-Physical memory block links (from LBA0/PBA0 to LBA7/PBA7). The Read BBM LUT command can be used to check the existing address links stored inside the LUT.

The Read BBM LUT command is initiated by shifting the instruction code “A5h” into the DI pin and followed by 8-bits dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bits “Logical Block Address” and the 16-bits “Physical Block Address” as illustrated in **Figure 29**. All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all “00h” data.

The MSB bits LBA [15:14] of each link are used to indicate the status of the link.

LBA[15] Enable	LBA[14] Invalid	Descriptions
0	0	This link is available to use
1	0	This link is enabled, and it is a valid link
1	1	This link was enabled, and it is a not valid link anymore
0	1	Not applicable

Figure 29 Read BBM LUT Sequence

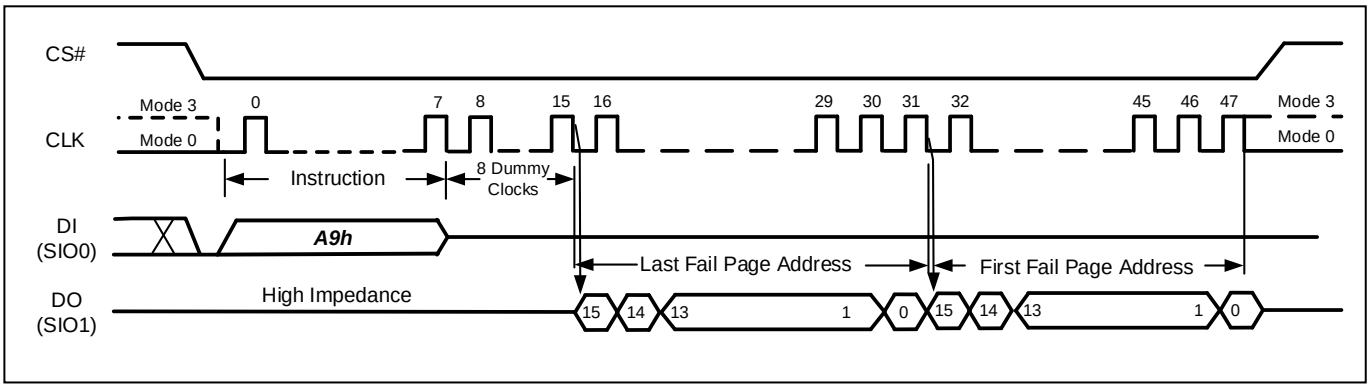


10.10.3 ECC Failure Page Address(A9h)

During the Read operations, ECC information will be used to verify the data read out from the physical memory array and possible corrections can be made to limited amount of data bits that contain errors. The ECC Status Bits (ECCS1-0) will also be set indicating the result of ECC calculation.

For the “Sequential/Continuous Read Mode (BUF=0)” operation, multiple pages of main array data can be read out continuously by issuing a single read command. Upon finishing the read operation, when ECC Enable Bit (ECC-E) is set to 1, the ECC status bits should be check to verify if there’s any ECC correction or un-correctable errors existed in the read out data. If ECCS1-0 equal to (1, 0) or (1, 1), the previous read out data contain one or more pages that contain ECC un-correctable errors. The first and last failure page address can be obtained by issuing the “ECC failure Page Address” command as illustrated in **Figure 30 Last ECC Failure Page Address Sequence**.

Figure 30 Last ECC Failure Page Address Sequence



11 Software Algorithm

11.1 Initial Invalid Block(s)

Invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same electrical characteristics. An initial invalid block(s) does not affect the performance of valid block(s). The system design must be able to mask out the initial invalid block(s) via address mapping. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.

N_{VB} represents the minimum number of valid blocks in the total number of available blocks (See the below table).

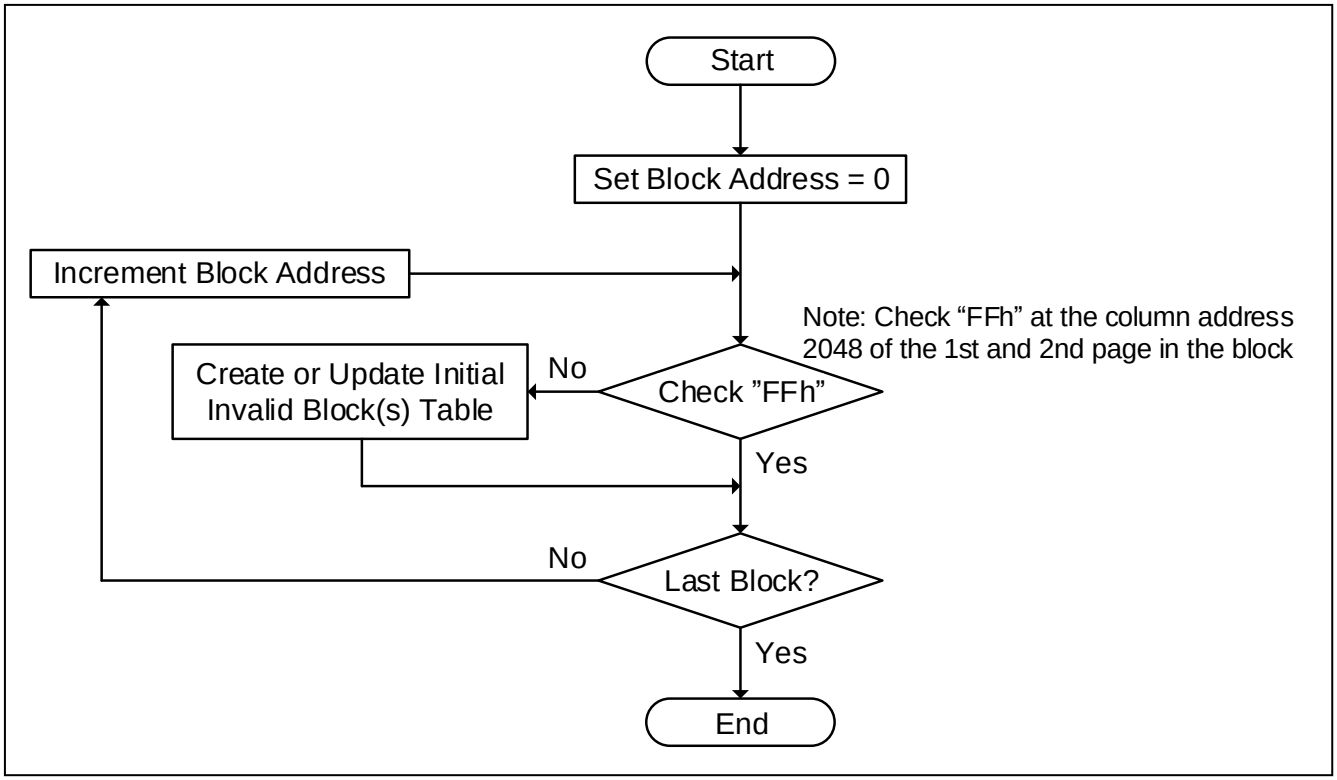
Table 19 Valid Block Number

Parameter	Symbol	Min	Max	Unit
Valid block number	N_{VB}	184	192	Blocks

11.2 Identifying Initial Invalid Block(s)

All device locations are erased (FFh) except locations where the initial invalid block(s) information is written prior to shipping. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the suggested flow (**Figure 31**). Any intentional erasure of the original initial invalid block information is prohibited.

Figure 31 Flow to Create Initial Invalid Block Table



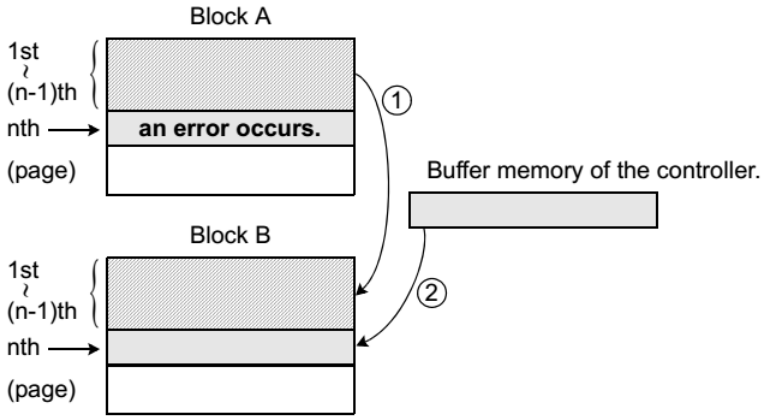
11.3 Error in Operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the blocks with correctable bit error reclaimed by ECC don’t need to be replaced. The said additional block failure rate does not include those reclaimed blocks.

Table 20 Failure Modes

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction

Figure 32 Bad Block Replacement



* Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

11.4 Internal ECC

The internal ECC logic may detect 2-bit error and correct 1-bit error in each ECC sector. An ECC segment is composed by a main area (512 Byte) and a spare area (16 Byte). The default state of the internal ECC is enabled. It is operated by the Set Feature operation to enable or disable internal ECC, and then check the internal ECC state by Get Feature operation.

The internal ECC is enabled by using Set Feature command (1Fh) to set ECC-E. To disable the internal ECC can be done by using the Set Feature command (1Fh) to clear ECC-E.

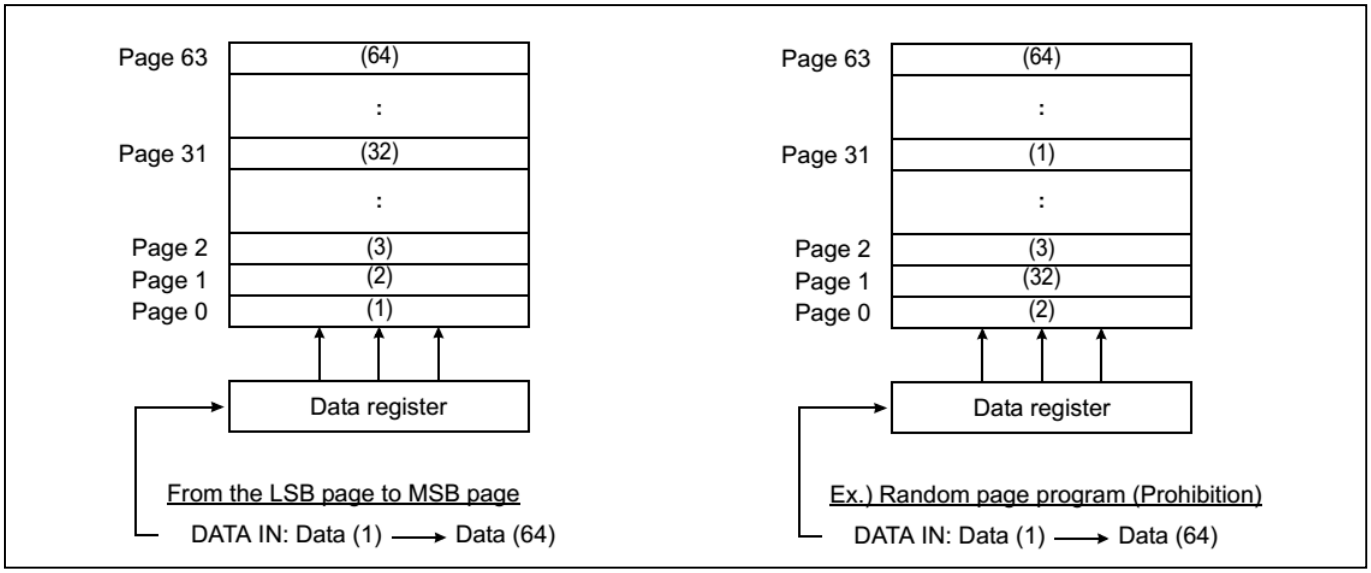
When the internal ECC is enabled:

- During a Program operation, an ECC code is calculated and stored in the additional spare area.
- During a Read operation, after the data transfer time (tRD_{ECC}) is completed, a Get Feature command should be issued to check the ECC status bits which indicate whether or not the error correction was successful. Please refer to **Status Register**. Furthermore, user could check the detailed bits error information for each ECC sector by Get Feature operation. See **Sector ECC Status Register** for details.
- The number of partial-page program is not 4 in an ECC sector, the user need to program the sector (528 Byte) at one program time, so the ECC parity code can be calculated properly.

11.5 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to the MSB (most significant bit) pages of the block. The LSB page is defined as the start page among the pages to be programmed, does not need to be page 0 in the block. Random page address programming is prohibited.

Figure 33 Addressing for Program Operation



12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Table 21 Absolute Maximum Rating

Parameters	Symbol	Range	Unit
Supply Voltage	V_{CC}	–0.6 to +4.6	V
Voltage Applied to Any Pin	V_{IO}	–0.6 to V_{CC}+0.4	V
Temperature under Bias	T_{BIAS}	–40 to +125	°C
Storage Temperature	T_{STG}	–65 to +150	°C
Short circuit output current, I/Os	I_{OS}	5	mA

Note:

(1) Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.

(2) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

12.2 Operating Ranges

Table 22 Operating Ranges

Parameters	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{CC}		2.7	3.6	V
Ambient Temperature	T_A	Industrial	-40	+85	°C
		Industrial plus	-40	+105	°C

12.3 Power-up and Power-down Timing Requirements

Table 23 Power-up Timing

Parameters	Symbol	Min	Max	Unit
V_{CC}(min) to read Status Register is allowed	t_{VSL}	200		µs
Time delay before device fully accessible	t_{PUW}	1		ms

Note:

(1) These parameters are characterized only.

Figure 34 Power-up Timing

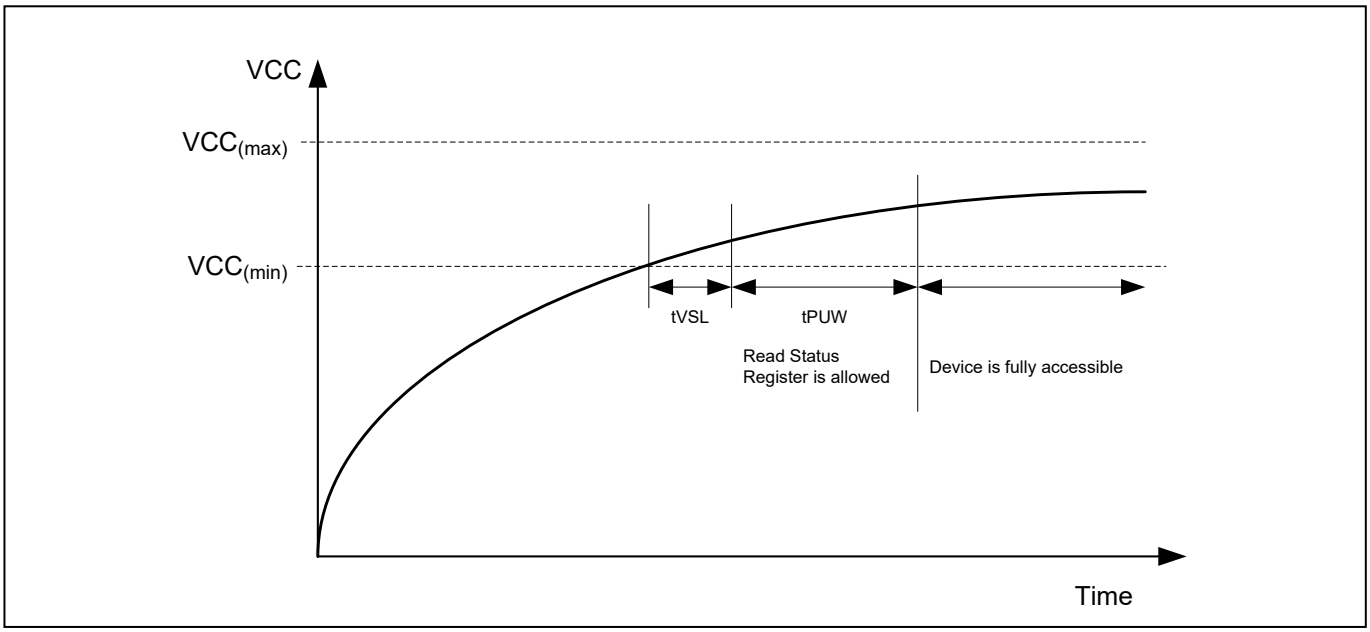
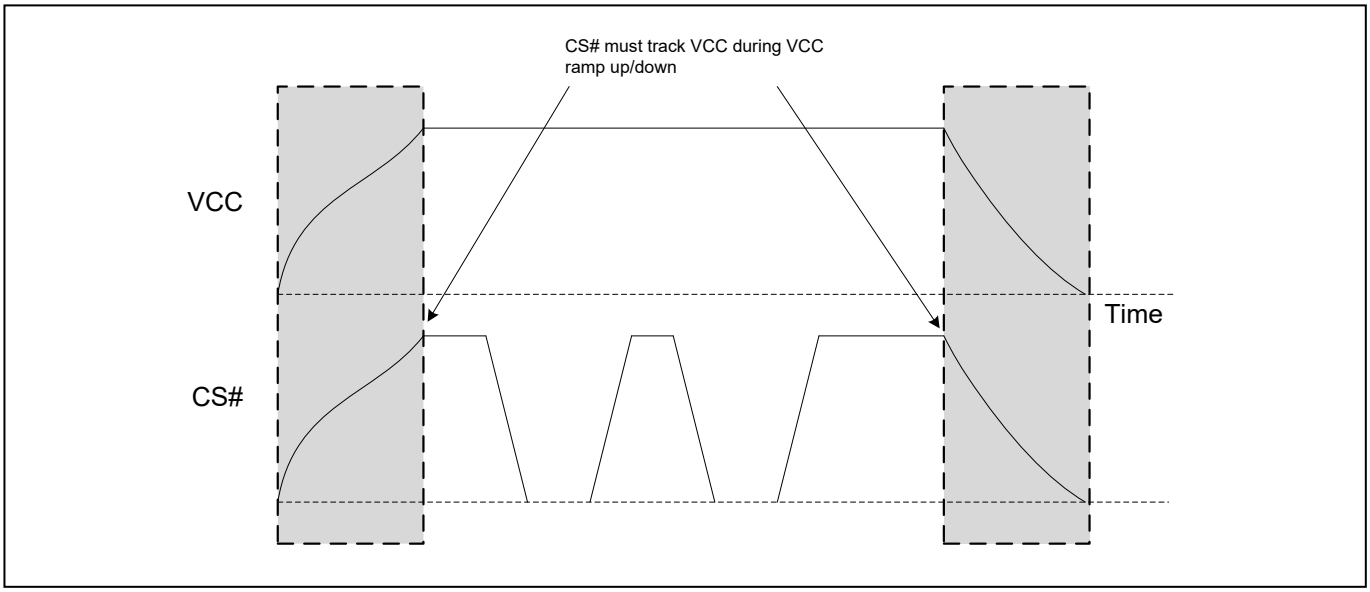


Figure 35 Power-up and Power-down Requirements



12.4 Pin Capacitance

Table 24 Pin Capacitance

Parameters	Symbol	Min	Max	Unit
Input / Output Capacitance	C_{IO}		8	pF
Input Capacitance	C_{IN}		8	pF

Note:

(1) Test conditions: TA=25°C, F=1MHz, V_{IN}=0V, V_{CC}=3V

(2) These parameters are characterized only.

12.5 DC Electrical Characteristics

Table 25 DC Electrical Characteristics

Parameters	Symbol	Conditions	SPEC(1)			Unit
			Min	Typ	Max	
Standby Current	I_{CC1}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		10	50	μA
Page Read Current	I_{CC2}			10	25	mA
Program Current	I_{CC3}			15	25	mA
Erase Current	I_{CC4}			15	25	mA
Input Leakage Current	I_{LI}				±2	μA
Output Leakage Current	I_{LO}				±2	μA
Input Low Voltage	V_{IL}		-0.3		$0.2V_{CC}$	V
Input High Voltage	V_{IH}		$0.8V_{CC}$		V_{CC}+0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = -400μA	2.4			V

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 2.7V to 3.6V, unless otherwise noted.

12.6 AC Measurement Conditions

Table 26 AC Measurement Conditions

Parameters	Symbol	Min	Max	Unit
Load Capacitance	C_L		30	pF
Input Rise Time	t_R		2.5	ns
Input Fall Time	t_F		2.5	ns
Input Pulse Voltages	V_{IN}	0 to V_{CC}		V
Input Timing Reference Voltages	IN	$0.5V_{CC}$		V
Output Timing Reference Voltages	OUT	$0.5V_{CC}$		V

12.7 AC Electrical Characteristics

Table 27 AC Electrical Characteristics

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
Clock frequency	F_R			166	MHz
Clock frequency for DTR	F_{RD}			83	MHz
Clock frequency for Sequential or Continuous Read with ECC e.g. BUF=0, ECC_E=1	F_{R1}			83	MHz
Clock frequency for Sequential or Continuous Read without ECC	F_{R2}			120	MHz

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
e.g. BUF=0, ECC_E=0					
Clock High, Low Time for all commands	t_{CLH}, t_{CLL}(2)	2.7			ns
Clock Rise Time	t_{CLCH}(4)	0.1			V/ns
Clock Fall Time	t_{CHCL}(4)	0.1			V/ns
Data In Setup Time	t_{DVCH}	2			ns
Data In Setup Time (DTR only)	t_{DVCL}	2			ns
Data In Hold Time	t_{CHDX}	3			ns
Data In Hold Time (DTR only)	t_{CLDX}	3			ns
Clock Low to Output Valid	t_{CLQV}(4)			5.5	ns
Clock High to Output Valid (DTR only)	t_{CHQV}			5.5	ns
Output Hold Time	t_{CLQX}	1			ns
Output Hold Time (DTR only)	t_{CHQX}	1			ns
Output Disable Time	t_{SHQZ}(3)			20	ns
CS# active Setup Time	t_{SLCH}	5			ns
CS# active Hold Time	t_{CHSH}	5			ns
CS# non-active Setup Time	t_{SHCH}	5			ns
CS# non-active Hold Time	t_{CHSL}	5			ns
CS# deselect Time	t_{SHSL}	20			ns
HOLD# active Setup Time	t_{HLCH}	5			ns
HOLD# active Hold Time	t_{CHHH}	5			ns
HOLD# non-active Setup Time	t_{HHCH}	5			ns
HOLD# non-active Hold Time	t_{CHHL}	5			ns
HOLD# to Output Low-Z	t_{HHQX}(3)			25	ns
HOLD# to Output High-Z	t_{HLQZ}(3)			25	ns
WP# Setup Time before CS# Low	t_{WHSL}	20			ns
WP# Hold Time after CS# Low	t_{SHWL}	100			ns
Device reset time (Read/Program/Erase)	t_{RST}(3)			5/20/200	µs
Sequential Page Read Stop to Device Ready Time	t_{RDSTOP}(3)			20	µs

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 2.7V to 3.6V, unless otherwise noted.

(2) $t_{CLH} + t_{CLL} <= 1/F_R$

(3) These parameters are characterized only.

(4) When BUF=0, max tCLQV is 5.8ns

12.8 Read / Program / Erase Characteristics

Table 28 Read / Program / Erase Characteristics

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
Data Transfer from Cell to Data Register	t_{RD}			25	µs
Data Transfer from Cell to Data Register with internal ECC enabled	t_{RD_ECC}		60	65	µs

Parameters	Symbol	SPEC(1)			Unit
		Min	Typ	Max	
Program Time	t_{PROG}(2)		350	700	μs
Program Time with internal ECC enabled	t_{PROG_ECC}(2)		390	750	μs
Block Erase Time	t_{ERS}		2	10	ms
Number of Partial Program Cycles	NOP			4	cycles

Note:

(1) Applicable over recommended operating range from: T_A = -40°C to +85°C, VCC= 2.7V to 3.6V, unless otherwise noted.

(2) Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V and 25°C.

(3) These parameters are characterized only.

13 Timing Diagram

Figure 36 Serial Input Timing

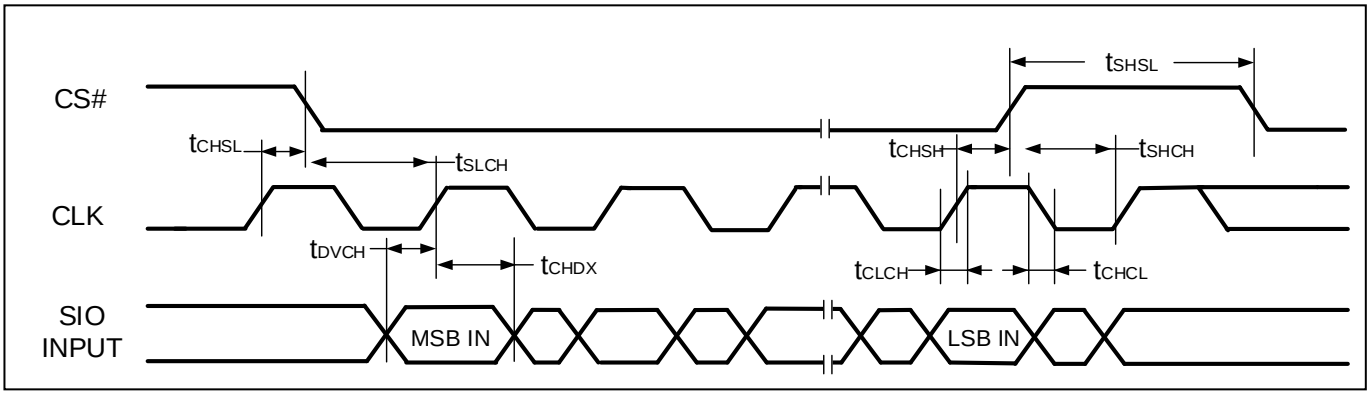


Figure 37 Serial Input Timing (DTR)

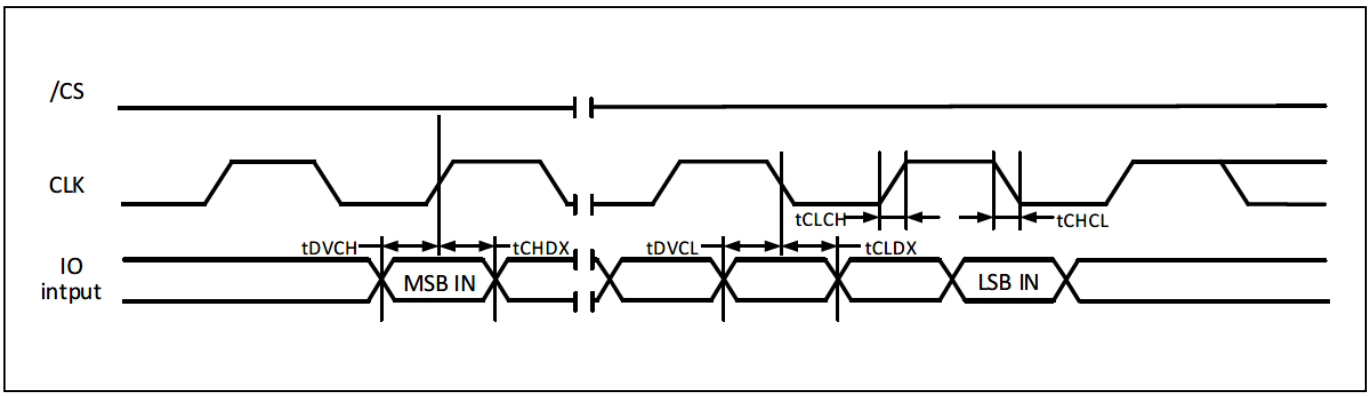


Figure 38 Serial Output Timing

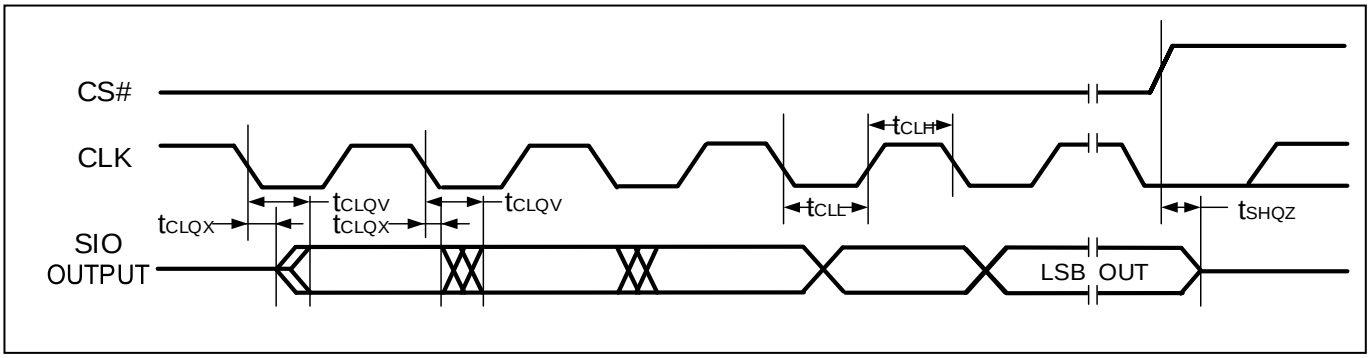


Figure 39 Serial Output Timing (DTR)

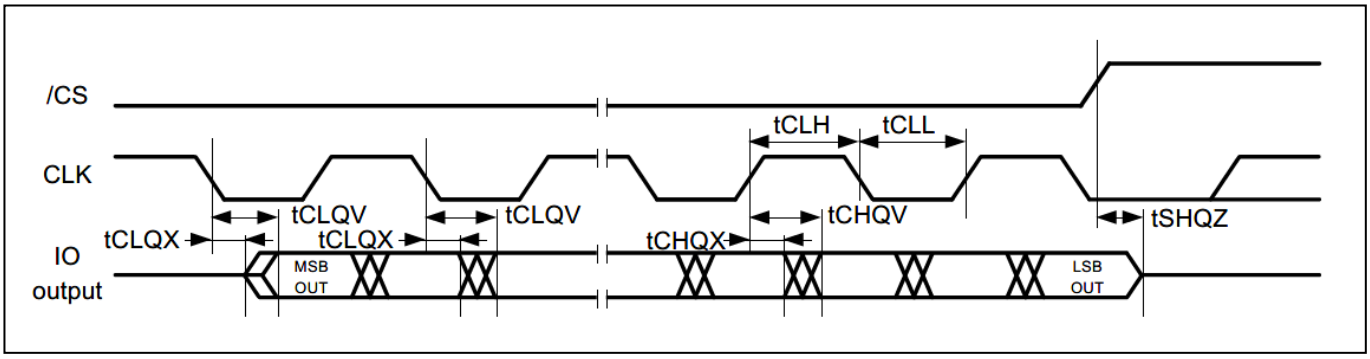


Figure 40 HOLD# Timing

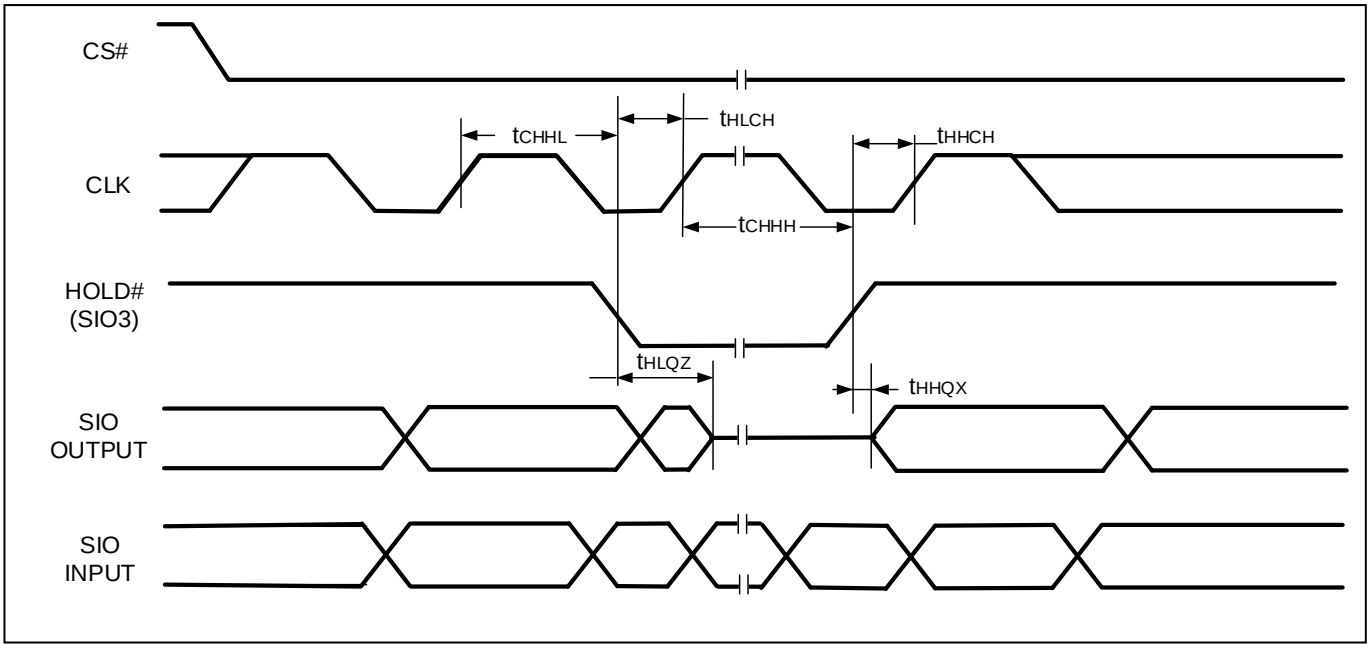
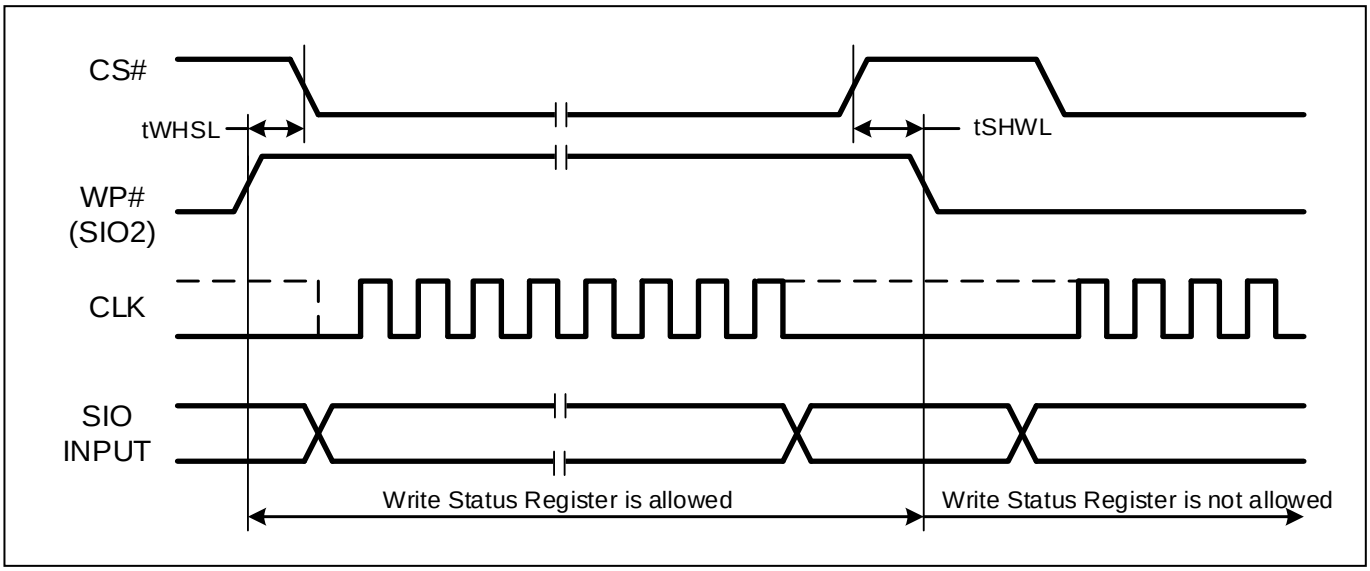
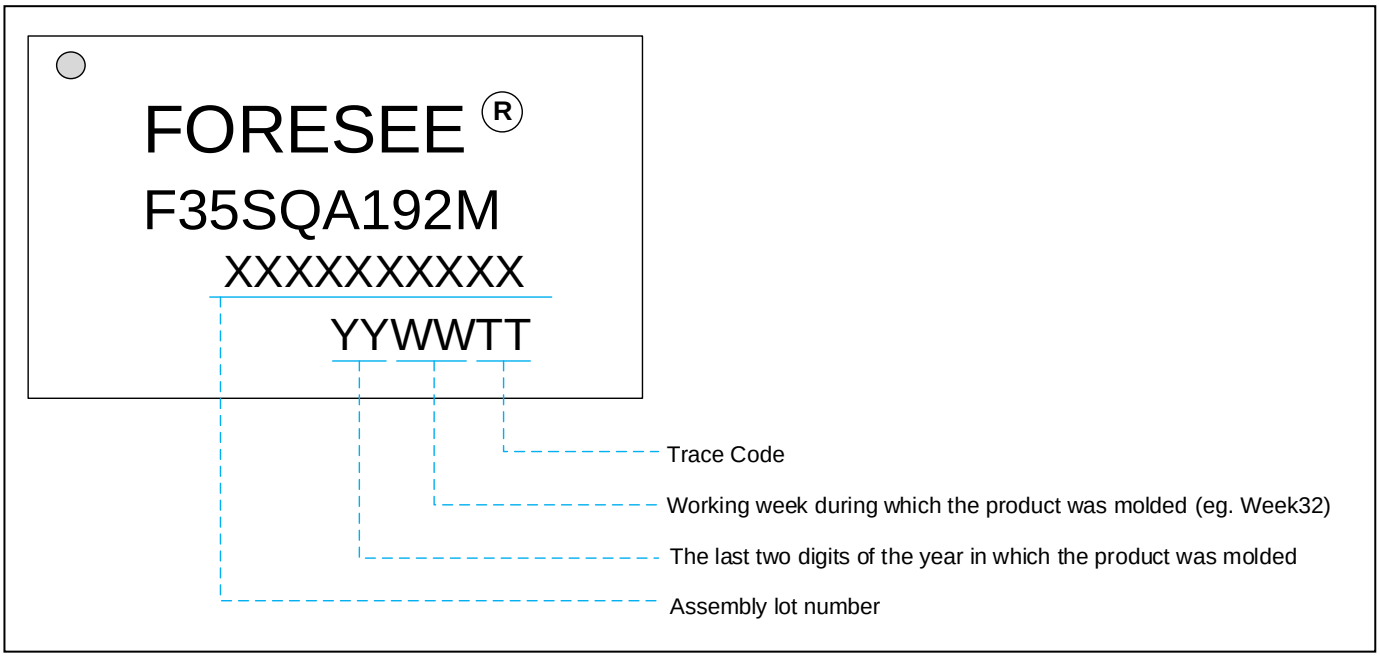


Figure 41 WP# Timing

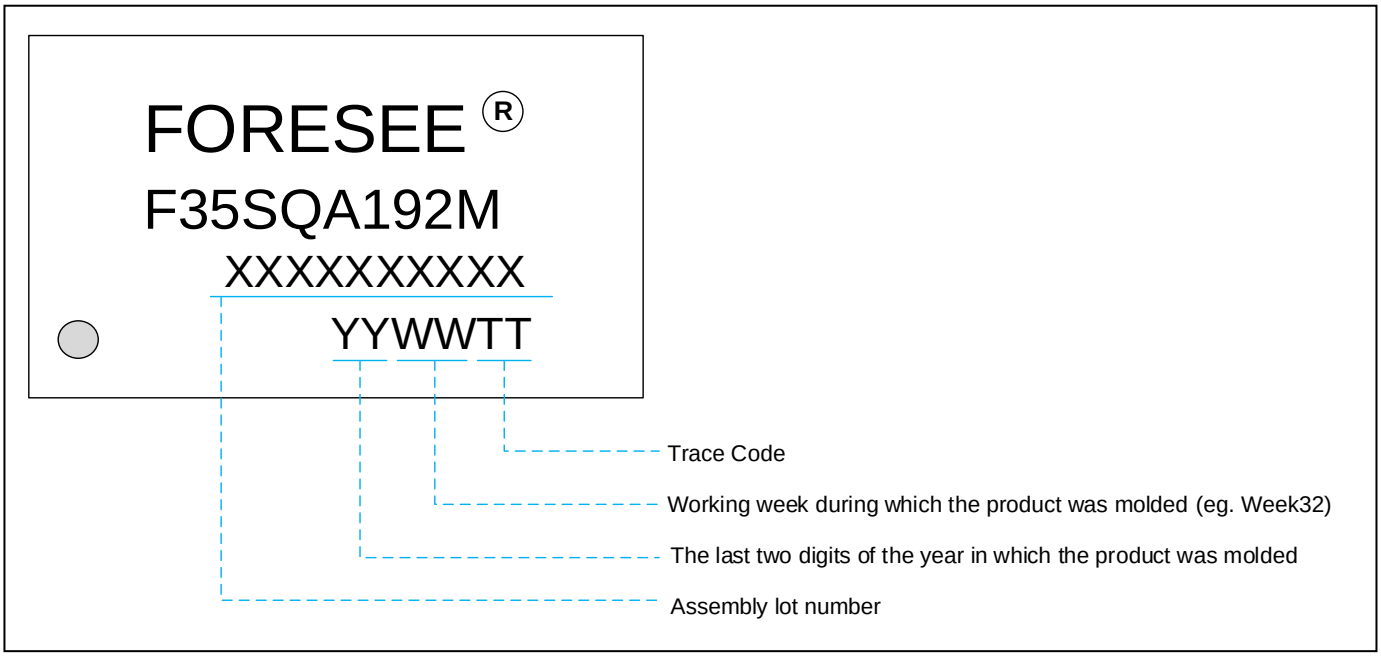


14 Part Marking Scheme

14.1 8-WSON (5x6mm)



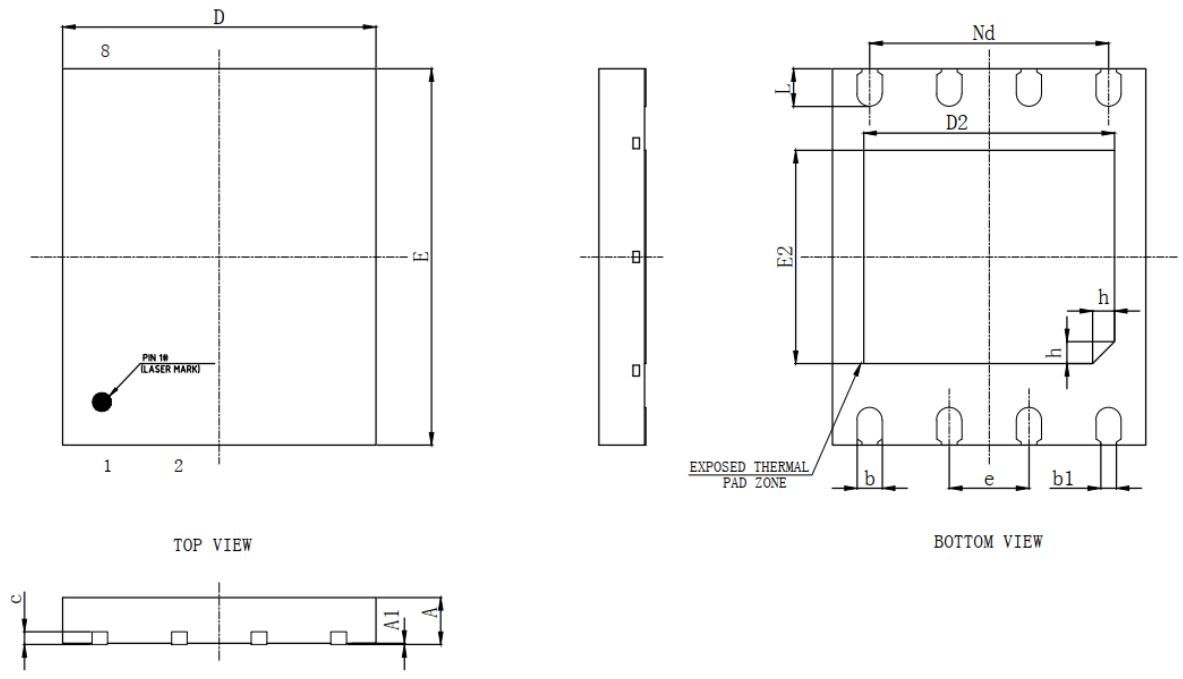
14.2 8-SOP(150mil & 208mil)



15 Packaging Information

15.1 8-WSON (5x6mm)

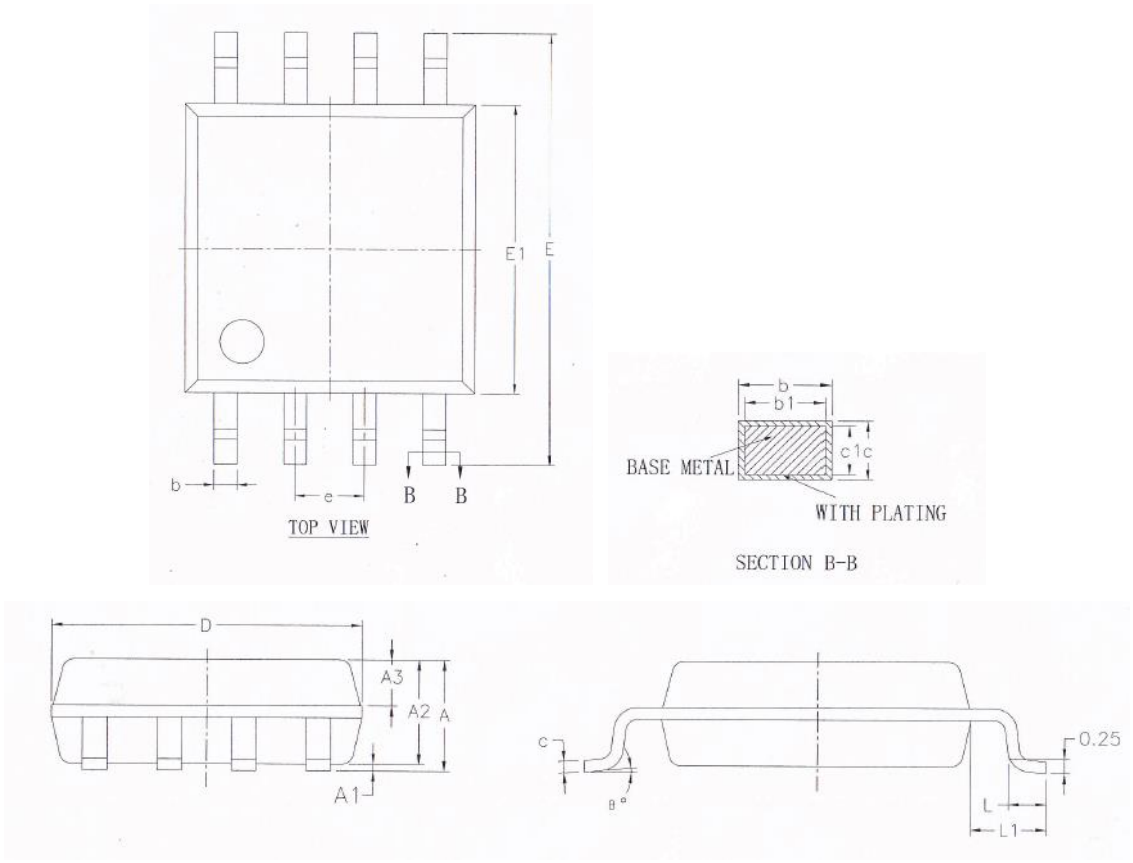
Figure 42 8-WSON (5x6mm) Package Information



SYMBOL	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
b1		0.25 REF.	
c	0.18	0.203	0.25
D	4.90	5.00	5.10
Nd		3.81 BSC	
e		1.27 BSC	
E	5.90	6.00	6.10
D2	3.90	4.00	4.10
E2	3.30	3.40	3.50
L	0.55	0.60	0.65
H	0.30	0.35	0.40

15.2 8-SOP (208mil)

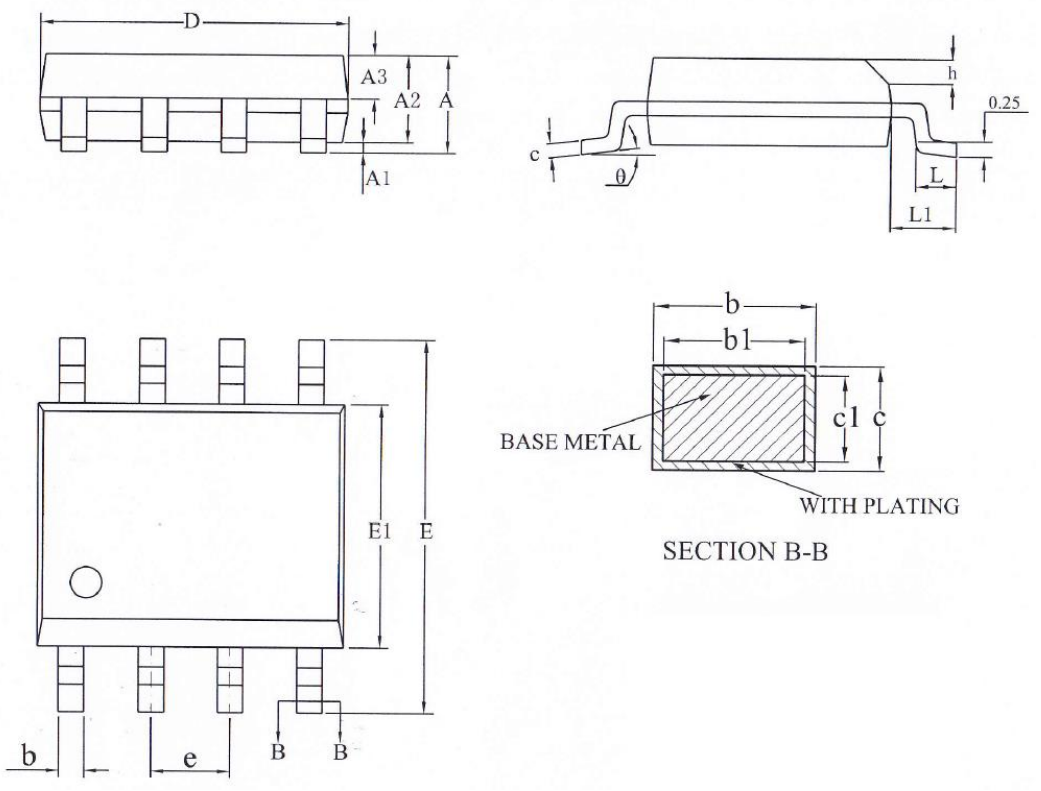
Figure 43 8-SOP (208mil) Package Information



SYMBOL	DIMENSION (mm)		
	Min.	Nom.	Max.
A	-	-	2.15
A1	0.05	-	0.25
A2	1.70	1.80	1.90
A3	0.75	0.80	0.85
b	0.31	-	0.50
b1	0.27	0.43	0.46
c	0.15	-	0.30
c1	0.15	0.20	0.25
D	5.13	5.23	5.33
E1	5.18	5.28	5.38
E	7.70	7.90	8.10
e	1.27 BSC		
L	0.50	0.65	0.80
L1	1.31 REF.		
θ	0°	-	8°

15.3 8-SOP (150mil)

Figure 44 8-SOP (150mil) Package Information



SYMBOL	DIMENSION (mm)		
	Min.	Nom.	Max.
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05 REF.		
θ	0°	-	8°