MEGAHUNT

MH1903S
Brief Introduction

Highly Integrated Secure SOC

Version: 2.0
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Megahunt Tehnologies Inc.

Revision Record

Date	Version	Description	Author
2020-01-03	1.00	Completed the first draft	MEGAHUNT
2020-02-23	1.10	Added the definition of QFN88 pin	MEGAHUNT
2020-03-24	1.20	Added the definition of QFN88_J pin	MEGAHUNT
2020-04-14	1.30	Modified the definition of QFN88 pin	MEGAHUNT
2020-04-30	1.40	Improved the block diagram information	MEGAHUNT
2020-05-08	1.50	Deleted excess packaging	MEGAHUNT
2020-05-18	1.60	Improved the electrical parameters	MEGAHUNT
2020-05-26	1.70	Adjusted PIN55/PIN56 pins in QFN88 packaging, deleted IO of magnetic track 1, ordinary IO instead	MEGAHUNT
2020-06-18	1.80	Modified the definition of QFN88 pin	MEGAHUNT
2020-08-04	1.90	Deleted the description of QFN88 PIN2 pin	MEGAHUNT
2020-11-20	2.00	1. Added the explanation to material code information 2. Modified the range of CHARGE_VCC voltage	MEGAHUNT

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1 Overview of Chip

1.1 Description of chip

With SC300 security core processor and the basic frequency up to 204MHz, MH1903S makes full use of its excellent architectural characteristics and the high performance so as to achieve the high performance and provide the safe and energy-saving solutions.

With the built-in security encryption module, the chip supports a variety of encryption security algorithms, including DES, TDES, AES, RSA, ECC, SHA, and other encryption algorithms. The chip hardware also supports a variety of attack detection functions, and conforms to the financial security equipment standards.

The chip contains the BOOT program, supporting the verification of firmware signature upon downloading and starting. In addition to the built-in 640KB SRAM, the chip also integrates abundant peripheral resources, including Smartcard, magnetic stripe card decoding, security keyboard, LCDI, DCMI, etc. All the peripheral driver software is compatible with the current mainstream security chip software interface and in line with ARM CMSIS specification. The users can develop and transplant quickly on the basis of the existing solutions.

1.2 Main functions and characteristics of chip

- ARM SecurCore™ SC300™ core
  - 32-bit RISC Core (ARMv7-M)
  - MPU memory protection unit
  - Maximum basic frequency of 204MHz (adjustable for 1 and 2 frequency division)
  - FPU unit
  - 1 controlled JTAG-DP/SW-DP debugging port
- 640KB SRAM
- 1 QSPI controller, supporting XIP
- System control module (To control all peripheral module clocks and system-related configurations)
- Security encryption algorithm accelerator engine
  - Symmetric algorithms: DES, TDES, AES-128/192/256
  - Asymmetric algorithm: RSA-1024/2048, ECC
  - HASH check algorithm: SHA-1/224/256/384/512
- 2 SmartCard interfaces (supporting EMV level-1 protocol specification, ISO7816-3 standard), where SCI0 integrates 7816 level conversion function, and can be configured with output of 3V and 1.8V
- 4 UART interfaces (Supporting 4 lines)
- 3 SPI interfaces (Where SPI0 can be configured as master and slave, the other 2 interfaces only support Master)
- 1 high-speed SPI Master interface SPI5

- 1 IIC interface
- 1 KBD (4x5 matrix keyboard)
- 8 32-bit TIMER (With PWM function, supporting single-cycle output)
- 1 LCDI interface, supporting 8080 and 6800 bus protocol
- 1 true random number generator
- 1 DMA controller (supporting 8-channel DMA transmission)
- 1 CRC module (Supporting 16Bit/32Bit, a variety of common polynomial calculation)
- Support up to 87 GPIOs
- Support up to 8 static Tampers or 4 groups of dynamic Tampers (4 outputs, 4 inputs), dynamic/static state configurable
- 1 group of internal Sensors (Supporting high and low voltage, high and low temperature, Mesh, clock and voltage glitch detection)
- 1 secret key storage area (Supporting rapid erase of hardware)
- 1 USB (OTG-FS)
  - Support USB2.0 and OTG1.0a
  - Built-in USB PHY module
  - Private interrupt vector, to accelerate the data communication speed
- Integrated internal watchdog
- 1 10-bit DAC interface
- 1 7-channel 12-bit ADC, supporting up to 857 KHz sampling rate (channel 0 used for acquisition of CHARGE_VBAT voltage, the other channels used for acquisition for voltage ranging from 0 ~ 1.8V of 0 ~ 3.6V, which are configurable).
- Support magnetic stripe decoding function, support the standard cards such as ISO/ABA, AAMVA, IBM and JIS II
- 1 DCMI interface
- The chip integrates a LDO with up to 150mA output current
- The chip integrates USB charging management module, supporting the maximum charging current of 200 mA
- The chip integrated the power-on/off function
- Support the output of 27.12M frequency

1.3 Applications of MH1903S

Standalone QR code scanning terminals

MPOS and other payment terminals with QR code scanning

Smart terminals

Micro printers

1.4 Description of basic structure of chip

MH1903S includes security core, 640 KB SRAM, system control module, security encryption module, true random number module, 18-channel DMA controller, 1 USB interface, 1 GPIO module, 1 WDT module, 1 BPU module, 8 32-bit Timer, 1 CRC module, 3 SPI interfaces, 1 high-speed SPI interface, 2 SCI interfaces, 4 UART interfaces, 1 DAC, 1 6-channel ADC, and 1 DCMI interface; the block diagram of the system is shown as follows:

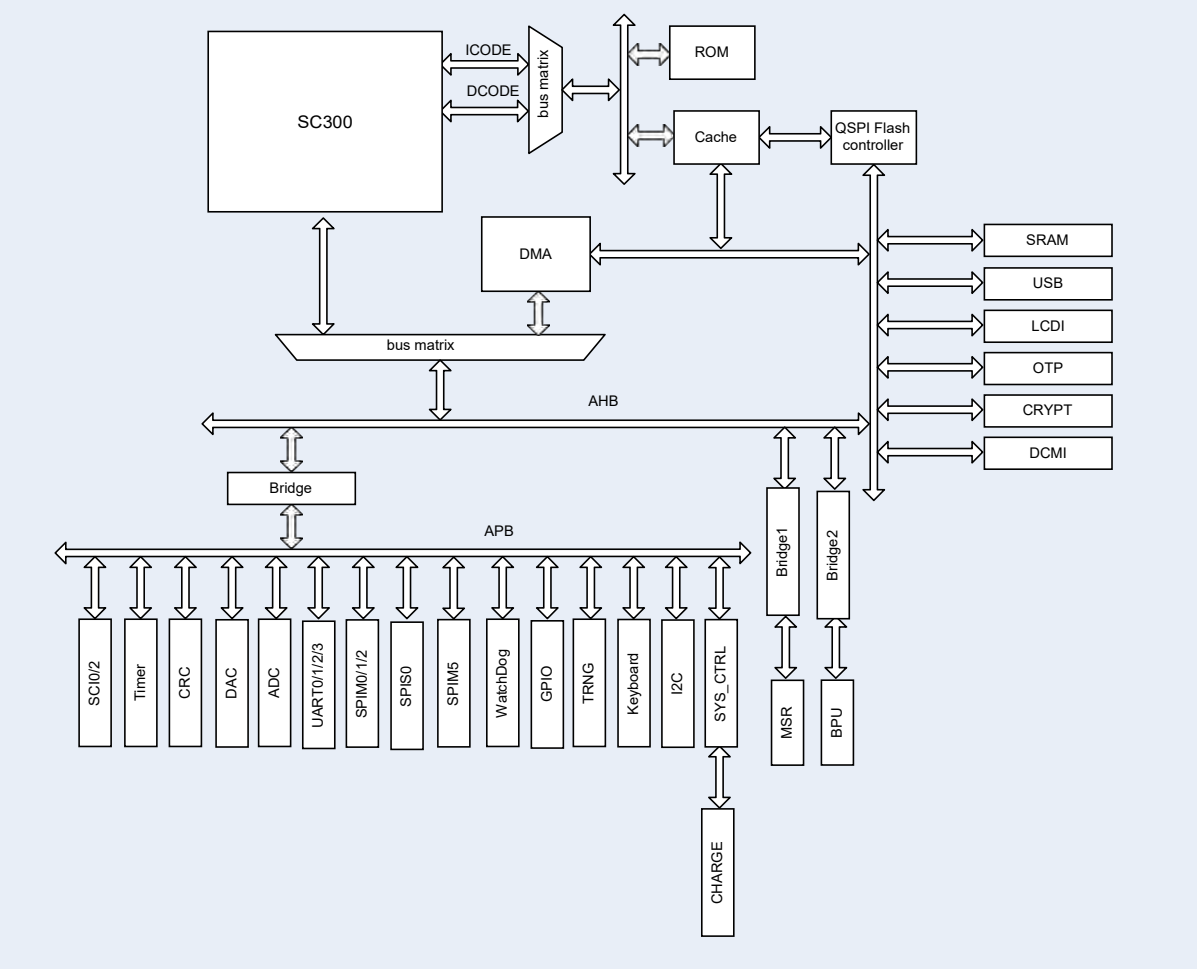


Figure 1 Main Modules of System

2 Characteristics of Chip

2.1 Electrical characteristics

Table 1 Ultimate Parameters

Parameters	Note	Range	Unit
Iddpd	Power-off current	--	nA
Tamb	Operating temperature	-40~+85	℃
Tstg	Storage temperature	-40~+125	℃
Ground	Ground	-0.3~0.3	V
Voh	Digital output high level	VDD -0.3 ~ VDD+0.3	V
Vol	Digital output low level	<0.4	V
Ioh	Source current (PA2/3/4/5, PC6/7/8/9)	27 (@3V)	mA
	Source current (other IO)	16 (@3V)	mA
Iol	Sink current (PA2/3/4/5, PC6/7/8/9)	27 (@0.5V)	mA
	Sink current (other IO)	16 (@0.5V)	mA
Vih	Digital input high level	≥0.7×VDD	V
ViL	Digital input low level	≤0.3×VDD	V

Table 2 Electrical Characteristics

Parameter	Condition (-40°C to +85°C)	Value		Unit
		Maximum	Minimum	
VCC		3.6	5.5	V
CHARGE_VCC		4.7	5.5	V
AVD33		2.7	3.6	V
VDD33		2.7	3.6	V
VBAT33		2	3.6	V
Vol	VDD=3.3V	-	0.4	V
Voh	VDD=3.3V	VDD – 0.3	-	V
VIH	VDD=3.3V	0.7×VDD	-	V
VIL	VDD=3.3V	-	0.3×VDD	V
Tamper input low level		-	0.3xVBAT33	V
Tamper input high level		0.7xVBAT33	-	V

Table 3 Safety-related Characteristics

Sensor	Note	Range	Unit
Temperature sensor	High temperature detection range	95~115	℃
	Low temperature detection range	-30~-45	℃
Voltage sensor	High voltage detection range of main power voltage	4.0±0.1	V
	Low voltage detection range of main power voltage	2.8±0.1	V
	High voltage detection range of battery voltage	4.0±0.1	V
	Low voltage detection range of battery voltage	1.9±0.1	V
Clock frequency sensor	12M clock frequency detection range	12±50%	MHz
	32K clock frequency detection range	32±50%	KHz
External Tamper resistance	Resistance of pull-up resistor on Tamper pin	7.5M±10%	Ω

Table 4 List of Power Consumptions

Operating Mode	Note	Power Consumption	Unit
RUN	● All peripherals are turned on		mA
	■ core 204MHz, HCLK 102MHz, PCLK 51MHz	67	
	■ core 192MHz, HCLK 96MHz, PCLK 48MHz	64	
	■ core 168MHz, HCLK 84MHz, PCLK 42MHz	59	
	● All peripherals are turned off		
	■ core 204MHz, HCLK 102MHz, PCLK 51MHz	43	
	■ core 192MHz, HCLK 96MHz, PCLK 48MHz	41	
	■ core 168MHz, HCLK 84MHz, PCLK 42MHz	38	
CPU Sleep	All peripherals are turned off 204@MHz	19	mA
Deep Sleep	● support IO low level wakeup	450	uA
VBAT	The Tamper pin is suspended during the test and the internal pulling resistor is turned on		uA
	● CHARGE_VBAT suspended		
	All internal sensors are turned on	2.1	
	All internal sensors are turned off	1.7	
	● CHARGE_VBAT connected to lithium battery		
	All internal sensors are turned on, 5.6uA@CHARGE_VBAT	0.7	
	All internal sensors are turned off, 5.6uA@CHARGE_VBAT	0.3	

2.2 Definitions of pins

2.2.1 QFN88_J

Table 5 Definitions of 5MH1903S QFN88_J 10mm×10mm Packaging Pins

PIN No.	PID Name	ALT0	ALT1 (default)	ALT2	ALT3	Remark
1	PA5		PA[5]	PWM5	CLK_24M	Output of 24M configurable
2	PA8	SCI0_CLK	PA[8]		SPI1_MOSI	In case of IO multiplexing, the IC card power must be turned on first, and the high level of the output signal is the IC card output level
3	PA9	SCI0_RSTN	PA[9]		SPI1_MISO	
4	PA10	SCI0_IO	PA[10]			
5	CVCC					IC card power supply
6	PA6	SCI0_DET	PA[6]	PWM6	SPI1_SCK	
7	VDD33					
8	PE6	UART3_CTS	PE[6]	I2C0_SCL		
9	PE7	UART3_RTS	PE[7]	I2C0_SDA		
10	PE8	SCI2_DET	PE[8]	UART3_RX		
11	PE9	SCI2_VCCEN	PE[9]	UART3_TX		
12	PE10	SCI2_CLK	PE[10]	UART3_CTS		
13	PE11	SCI2_RSTN	PE[11]	UART3_RTS		
14	PE12	SCI2_IO	PE[12]			
15	PA0	UART0_RX	PA[0]	PWM0		
16	PA1	UART0_TX	PA[1]	PWM1		
17	PA2	UART0_CTS	PA[2]	PWM2	I2C0_SCL	
18	PA3	UART0_RTS	PA[3]	PWM3	I2C0_SDA	
19	PB0	I2C0_SCL	PB[0]	PWM0	XTAL32K	
20	PB1	I2C0_SDA	PB[1]	PWM1	CLK_24M	
21	PB2	SPI2_SCK	PB[2]	PWM2	UART2_RX	
22	PB3	SPI2_CSN	PB[3]	PWM3	UART2_TX	
23	PB4	SPI2_MOSI	PB[4]	PWM4	UART2_CTS	
24	PB5	SPI2_MISO	PB[5]	PWM5	UART2_RTS	
25	PD1		PD[1]		DCMIS_DATA0	
26	PD2		PD[2]		DCMIS_DATA1	
27	PD3		PD[3]		DCMIS_DATA2	
28	PD8		PD[8]	UART2_RX	DCMIS_DATA3	
29	PD9		PD[9]	UART2_TX	DCMIS_DATA4	
30	PD10		PD[10]	KeyBoard7	DCMIS_DATA5	
31	PD11		PD[11]	KeyBoard8	DCMIS_DATA6	
32	PE0		PE[0]	KeyBoard4	DCMIS_DATA7	
33	PD6	UART1_CTS	PD[6]		DCMIS_DATA8	
34	PD7	UART1_RTS	PD[7]		DCMIS_DATA9	
35	PC6		PC[6]	PWM4	DCMIS_DATA10	
36	PC7		PC[7]	PWM5	DCMIS_DATA11	
37	PC8		PC[8]	PWM6	DCMIS_DATA12	
38	PC9		PC[9]	PWM7	DCMIS_DATA13	
39	PE1		PE[1]	KeyBoard5	DCMIS_VSYNC	
40	PE2		PE[2]	KeyBoard6	DCMIS_HSYNC	

41	PE3		PE[3]		DCMIS_PIX_CLK	
42	PB12	SPI0_CLK	PB[12]	PWM3	UART1_RX	
43	PB13	SPI0_CSN	PB[13]	PWM4	UART1_TX	
44	PB14	SPI0_MOSI	PB[14]	PWM5	UART1_CTS	
45	PB15	SPI0_MISO	PB[15]	PWM6	UART1_RTS	
46	VDD33					
47	PB11	SPI1_MISO	PB[11]	SCI2_IO	UART3_RTS	
48	PB10	SPI1_MOSI	PB[10]	SCI2_RSTN	UART3_CTS	
49	PB9	SPI1_CSN0	PB[9]	SCI2_CLK	UART3_TX	
50	PB8	SPI1_SCK	PB[8]	SCI2_VCCEN	UART3_RX	
51	PC11		PC[11]	XTAL32K		
52	PC12		PC[12]	SPI0_SCK	SPI5_MISO	SPI5 is a high-speed SPI
53	PC13		PC[13]	SPI0_CSN0	SPI5_MOSI	
54	PC14		PC[14]	SPI0_MOSI	SPI5_CSN	
55	PC15		PC[15]	SPI0_MISO	SPI5_CLK	
56	MSR_IN3					Magnetic strip card T2+
57	MSR_IN4					Magnetic strip card T2-
58	MSR_IN5					Magnetic strip card T3+
59	MSR_IN6					Magnetic strip card T3-
60	VDD33					
61	PC4	TCK	PC[4]	ADC_IN5	XTAL32K	
62	PC3	TMS	PC[3]	ADC_IN4	UART1_RTS	
63	PC2	TDO	PC[2]	ADC_IN3	UART1_CTS	
64	PC1	TDI	PC[1]	ADC_IN2/DAC	UART1_TX	
65	PC0	TRST	PC[0]	ADC_IN1	UART1_RX	Channel 1 does not support 5V
66	REFP					Connect 1uF earth capacitance
67	VDD25					Connect 1uF earth capacitance
68	PE14	KeyBoard5	PE[14]			
69	PE13	KeyBoard4	PE[13]			
70	PD0		PD[0]		CLK_27P12	Output of 27.12M configurable
71	PB6		PB[6]	PWM6	CLK_27P12	Output of 27.12M configurable
72	DN					USB DN
73	DP					USB DP
74	VBUS					USB VBUS
75	PF6	CLK_24M	PF[6]	PWM5		
76	PA11	SCI2_DET	PA[11]		CLK_24M	
77	VDD33					
78	VDD12					
79	AVD33					
80	XI32					XTAL 32K Input
81	XO32					XTAL 32K Output
82	EXT5					External Tamper5
83	EXT4					External Tamper4
84	EXT3					External Tamper3

85	EXT2					External Tamper2
86	EXT1					External Tamper1
87	EXT0					External Tamper0
88	VBAT33					Battery-powered supply must supply power; otherwise the chip cannot work

Differences with MH1903 QFN88:

1), PIN5: Internal integrated IC card level conversion, supporting the level of 3V and 1.8V

2), PIN65: ADC channel 0 is used for acquisition of CHARGE_VBAT voltage (0~5V), PC0 is changed to channel 1, and does not support 5V

3) Multiplexing adjustment of some IO functions, marked with yellow and red background colors

2.2.2 QFN88

Table 6 Definitions of MH1903S QFN88 10mm×10mm Packaging Pins

PIN No.	PID Name	ALT 0	ALT1 (default)	ALT2	ALT3	Remark
1	CVCC					IC card power supply
2	VDD33					
3	VCC					5V converted to 3.3V LDO input
4	VDD33_OUT					5V converted to 3.3V output
5	POWER_KEY					Power-on/off key
6	PA7	SCI0_VCCEN	PA[7]	PWM7	SPI1_CSN	
7	PA6	SCI0_DET	PA[6]	PWM6	SPI1_SCK	
8	PB2	SPI2_SCK	PB[2]	PWM2	UART2_RX/IrDA_IN	
9	PB3	SPI2_CSN	PB[3]	PWM3	UART2_TX/IrDA_OUT	
10	PB4	SPI2_MOSI	PB[4]	PWM4	UART2_CTS	
11	PB5	SPI2_MISO	PB[5]	PWM5	UART2_RTS	
12	PE6	UART3_CTS	PE[6]	I2C0_SCL		
13	PE7	UART3_RTS	PE[7]	I2C0_SDA		
14	PE8		PE[8]	UART3_RX/IrDA_IN		
15	PE9		PE[9]	UART3_TX/IrDA_OUT		
16	PE10		PE[10]	UART3_CTS		
17	PE11		PE[11]	UART3_RTS		

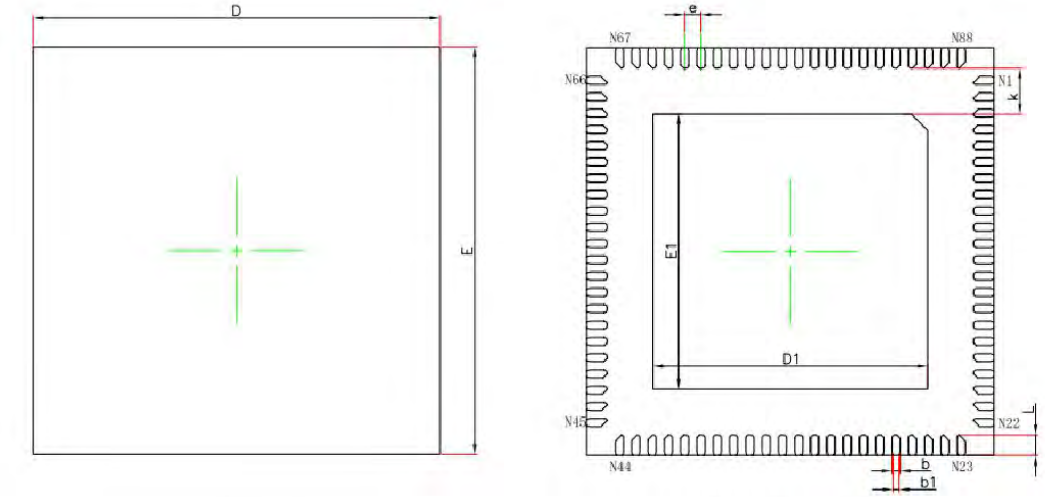
18	PA0	UART0_RX/IrDA_IN	PA[0]	PWM0		UART download pin
19	PA1	UART0_TX/IrDA_OUT	PA[1]	PWM1		
20	PA2	UART0_CTS	PA[2]	PWM2	I2C0_SCL	
21	PA3	UART0_RTS	PA[3]	PWM3	I2C0_SDA	
22	PB0	I2C0_SCL	PB[0]	PWM0	XTAL32K	
23	PB1	I2C0_SDA	PB[1]	PWM1	CLK_24M	Output of 24M configurable
24	CHARGE_VBAT					CHARGE power output, connect battery
25	CHARGE_VCC					CHARGE power input
26	PD1		PD[1]		DCMIS_DATA0	
27	PD2		PD[2]		DCMIS_DATA1	
28	PD3		PD[3]		DCMIS_DATA2	
29	PD8		PD[8]	UART2_RX/IrDA_IN	DCMIS_DATA3	
30	PD9		PD[9]	UART2_TX/IrDA_OUT	DCMIS_DATA4	
31	PD10		PD[10]	KeyBoard7	DCMIS_DATA5	
32	PD11		PD[11]	KeyBoard8	DCMIS_DATA6	
33	PE0		PE[0]	KeyBoard4	DCMIS_DATA7	
34	PD6	UART1_CTS	PD[6]		DCMIS_DATA8	
35	PD7	UART1_RTS	PD[7]		DCMIS_DATA9	
36	PC6		PC[6]	PWM4	DCMIS_DATA10	
37	PC7		PC[7]	PWM5	DCMIS_DATA11	
38	PC8		PC[8]	PWM6	DCMIS_DATA12	
39	PC9		PC[9]	PWM7	DCMIS_DATA13	
40	PE1		PE[1]	KeyBoard5	DCMIS_VSYNC	
41	PE2		PE[2]	KeyBoard6	DCMIS_HSYNC	
42	PE3		PE[3]		DCMIS_PIX_CLK	
43	PB12	SPI0_CLK	PB[12]	PWM3	UART1_RX/IrDA_IN	
44	VSS					Chip ground
45	PB13	SPI0_CSN	PB[13]	PWM4	UART1_TX/IrDA_OUT	
46	PB14	SPI0_MOSI	PB[14]	PWM5	UART1_CTS	
47	PB15	SPI0_MISO	PB[15]	PWM6	UART1_RTS	
48	PC12		PC[12]	SPI0_SCK	SPI5_MISO	
49	PC13		PC[13]	SPI0_CSN	SPI5_MOSI	

50	PC14		PC[14]	SPI0_MOSI	SPI5_CSN	
51	PC15		PC[15]	SPI0_MISO	SPI5_CLK	
52	VDD33					
53	PD13	UART2_TX/IrDA_OU T	PD[13]	KeyBoard1		
54	PD12	UART2_RX/IrDA_I N	PD[12]	KeyBoard0		
55	PD15	UART2_RTS	PD[15]	KeyBoard3		
56	PD14	UART2_CTS	PD[14]	KeyBoard2		
57	MSR_IN3					Magnetic strip card T2+
58	MSR_IN4					Magnetic strip card T2-
59	MSR_IN5					Magnetic strip card T3+
60	MSR_IN6					Magnetic strip card T3-
61	REFP					Connect 1uF earth capacitance
62	PC5		PC[5]	ADC_IN6	CLK_27P12	Output of 27.12M configurable
63	PC4	TCK	PC[4]	ADC_IN5	XTAL32K	
64	PC3	TMS	PC[3]	ADC_IN4	UART1_RTS	
65	PC1	TDI	PC[1]	ADC_IN2/DAC	UART1_TX/IrDA_OU T	
66	PC0	TRST	PC[0]	ADC_IN1	UART1_RX/IrDA_I N	
67	VDD25					Connect 1uF earth capacitance
68	DN					USB DN
69	DP					USB DP
70	VBUS					USB VBUS
71	VDD33					
72	XO12M					XTAL 12MHz Output
73	XI12M					XTAL 12MHz Input
74	VDD12					Connect 1uF earth capacitance
75	AVD33					
76	XI32					XTAL 32KHz Input
77	XO32					XTAL 32KHz Output
78	EXT5					External Tamper5
79	EXT4					External Tamper4
80	EXT3					External Tamper3
81	EXT2					External Tamper2
82	EXT1					External Tamper1

83	EXT0					External Tamper0
84	VBAT33					Button battery
85	PA5		PA[5]	PWM5	CLK_24M	Output of 24M configurable
86	PA8	SCI0_CLK	PA[8]		SPI1_MOSI	In case of IO multiplexing, the IC card power must be turned on first, and the high level of the output signal is the IC card output level
87	PA9	SCI0_RSTN	PA[9]		SPI1_MISO	
88	PA10	SCI0_IO	PA[10]			

2.3 Information on packaging

2.3.1 QFN88



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	9.900	10.100	0.390	0.398
E	9.900	10.100	0.390	0.398
D1	6.650	6.850	0.262	0.270
E1	6.650	6.850	0.262	0.270
k	1.125REF.		0.044REF.	
b	0.150	0.250	0.006	0.010
b1	0.150REF.		0.006REF.	
e	0.400BSC.		0.016BSC.	
L	0.400	0.600	0.016	0.024

Figure 2 MH1903S QFN88 10mm*10mm Packaging Dimension

2.4 Ordering Information on part numbers

Table 7 MH1903S part numbers

Ordering Information (Part Numbers)	SRAM	Flash	Embedded QR Scanning Algorithm	Definition of Pin
MH1903SQ8GMHJS	640KB	1MB	Standard	QFN88_J
MH1903SQ8GMH0S	640KB	1MB	Standard	QFN88
MH1903SQ8GNH0S	640KB	4MB	Standard	QFN88

3 Details of Functional Modules of MH1903S

3.1 Description of peripherals

3.1.1 SPI

The chip provides 1 SPI master/slave and 2 SPI master device interfaces, which can support communication with multiple slave devices when used as the master device interface.

Characteristics of SPI peripherals:

- Operation of Master mode and Slave mode at independent address
- Master mode supports full duplex, simplex receiving, simplex transmitting, EEPROM mode
- Multiple Master conflict detections
- Support three communication modes including Motorola SPI, Texas Instruments SPI, and National Semiconductor Microwire
- Receive and transmit FIFO independently at the depth of 16 and the fixed width of 16 bits
- The frame length is configurable, ranging from 4 to 16 bits
- DMA interface

The common Motorola SPI communication protocol supports four communication modes, so as to achieve full duplex communication. The default mode 0 is used to power on the system.

The 4 communication formats as specified in SPI protocol are described as follows:

- Mode 0: Clock polarity (CPOL) = 0, clock phase (CPHA) = 0. In this mode, the idle state of the serial synchronous clock is low level, and the chip will take sample at the first jump edge (rising edge) of the serial synchronous clock. The chip defaults to this mode.
- Mode 1: Clock polarity (CPOL) = 0, clock phase (CPHA) = 1. In this mode, the idle state of the serial synchronous clock is low level, and the chip will take sample at the second jump edge (falling edge) of the serial synchronous clock.
- Mode 2: Clock polarity (CPOL) = 1, clock phase (CPHA) = 0. In this mode, the idle state of the serial synchronous clock is high level, and the chip will take sample at the first jump edge (rising edge) of the serial synchronous clock.
- Mode 3: Clock polarity (CPOL) = 1, clock phase (CPHA) = 1. In this mode, the idle state of the serial synchronous clock is high level, and the chip will take sample at the second jump edge (rising edge) of the serial synchronous clock.

Note: In order to ensure the normal operation of the chip SPI, keep the CSN signal line at the high level during the process of mode switching.

At the same time, if the master thinks that there is an error in the slave during the process of communication, the slave can return to normal by raising the CSN.

SPI interfaces are described as follows:

- SCK: The clock input pin of SPI; when the communication rate of 200K is adopted, the delay of 20us is needed between the bytes as a minimum;
- CSN: The chip selection signal of SPI, which is the input pin of the chip, with low efficiency;
- MOSI: The data input pin of SPI;
- MISO: The data output pin of SPI.

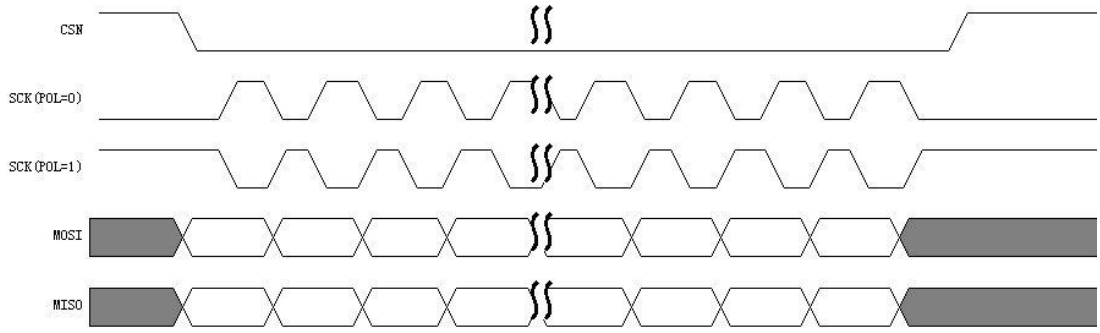


Figure 3 SPI Time Sequence 1 (CPHA=0)

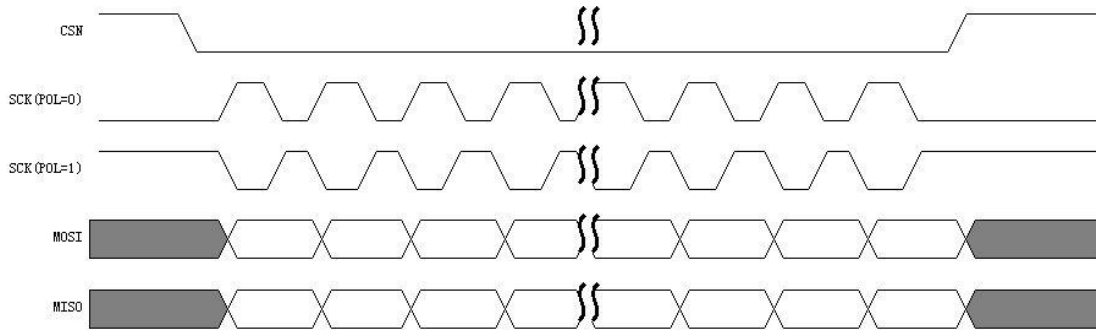


Figure 4 SPI Time Sequence 2 (CPHA=1)

3.1.2 High-speed SPI

The chip provides a high-speed SPI master interface, supporting the communication with multiple slave devices.

Characteristics of SPI peripherals:

- The Master mode supports the full duplex mode
- Receive and transmit FIFO with independent hardware, and the interrupt threshold for receiving and transmitting FIFO is configurable
- Receive and transmit FIFO at the depth of 64
- DMA interface

The common Motorola SPI communication protocol supports four communication modes, so as to achieve the full duplex communication. The default mode 0 is used to power on the system.

3.1.3 UART

The chip has four full-duplex UART serial communication interfaces, all of which support 4-wire mode

Characteristics of UART peripherals:

- Receive and transmit FIFO independently at the depth of 16 bytes
- Control of FIFO enabling
- Setting of data bits, supporting 5-8bit
- Forced output of 9 check bits
- Frame error, check error, break interrupt detection
- IrDA 1.0 IR protocol support
- DMA receiving

UART peripherals support independent receiving and transmitting of FIFO, and FIFO function can be configured for use by enabling bits.

The receiving and transmitting of FIFO by UART supports the full interrupt in receiving FIFO and the empty interrupt in transmitting FIFO respectively, and the trigger values thereof are configurable. The interrupt source in transmitting FIFO shares the same interrupt source with the transmitter holding register empty (THRE) in the non-FIFO mode, which is set by the software.

3.1.4 I2C

The chip provides 1 I2C master/slave interface. As a master device interface, it can support the communication with multiple slave devices.

Characteristics of I2C peripherals:

- Select I2C master or slave mode
- Support 7-bit/10-bit mode
- Support the speed in Standard mode and Fast mode
- Receive and transmit FIFO independently at the depth of 8 bytes
- SDA setting and holding time is adjustable
- Multi-master bus arbitration detection
- Support active termination of transmission
- Setting of glitch removal (Fast mode)
- DMA support

3.1.5 SCI

The chip supports up to two smart card interfaces, supporting ISO7816-3 standard and EMV Level-1 specification.

- Support the asynchronous T=0 and T=1 transmission protocols
- The timing sequence and the time parameters of the protocol are configurable
- Receiving and transmitting buffer at depth of 8 characters
- Receiving and transmitting FIFO monitor interrupt
- Interrupt status register
- When the detection card is removed, the hardware is automatically triggered to activate the timing sequence
- The deactivation timing sequence configurable by software
- Limited support for synchronization cards (control of input and output by register)

The external clock provided by SCI module F = PCLK/2 (SCICLKICC + 1), SCICLKICC bit width is 8bit, ranging from 0 to 255.

3.1.6 USB

OTG_FS controller interface, conforming to USB 2.0 standard and OTG 1.0a specification

- Support USB2.0
- Support OTG1.0a
  - Identify the inserted A-B type devices (ID)
  - Support the host negotiation protocol (HNP) and the session request protocol (SRP)
  - In OTG application, the host is allowed to shut down VBUS to save the power consumption
- Support USB full-speed/low-speed devices (type-B devices) under SRP protocol
  - Support USB full-speed/low-speed devices (type-A devices) under SRP protocol
  - USB OTG full-speed/low-speed dual-role device
- Provide 512-byte private RAM and advanced FIFO management

- RAM Configure different RAM areas for different FIFOs by the software, so as to make flexible and effective use of RAM
- Each FIFO can store multiple packets
- The dynamic allocation of storage areas is allowed
- The length of FIFO is not limited (The length with a power of 2 is not forced, and the memory area can be used continuously)
- The same endpoint number is allowed (IN/OUT endpoints share the same FIFO for more efficient use of the memory area)

- The maximum data flow of one frame (1ms) can be guaranteed without system intervention
- With a private DMA channel and the proprietary interrupt vector, the data communication can be accelerated
- Host mode
  - Supports up to 8 host channels, each of which can be dynamically configured for any type of transmission
  - Support up to 8 interrupt and synchronous transmission requests in the periodic hardware transmission request queue
  - Support up to eight transmission requests for control and high capacity transmission in the non-periodic hardware transmission request queue

3.1.7 BPU & Sensor

The built-in BPU module provides BPK unit, Sensor unit and RTC unit.

The BPK unit is powered by the onboard button battery , thus in the case of the failure of the external power supply won't cause the loss of the data in the BPK unit. When the Sensor unit detects an attack, the BPK shall be cleared by the BPK register settled.

Characteristics of sensor:

●Programmable external attack, support external static and external dynamic mode; in external static mode, up to 8 detection sources can be programmed; in external dynamic mode, up to 4 pairs of detection sources can be programmed.

●Internal attack detection includes 32K clock frequency detection, high and low temperature attack detection, and high and low voltage attack detection.

●Active shielding.

- Battery voltage glitch detection.

3.1.8 GPIO

The chip supports up to 87 GPIOs, and each IO multiplexes the pins with peripherals. Each GPIO can be configured as input, output, and interrupt mode; when GPIO is configured as output, each IO output value can be configured separately. IO supports strong push-pull/open-drain output modes.

3.1.9 True random number

With the built-in true random number generator, the user can obtain up to 128 bits of true random number at one time.

3.1.10 LCD controller interface (LCDI)

This Module is used to connect the "LCD Module" outside the chip, so as to communicate with 8080 or 6800 interface of the "LCD Module". The key characteristics include:

- Supports 4/8-bit interfaces on 8080 and 6800. 4-bit mode will execute two 4-bit read/write timing sequences in a row;
- 8080 or 6800 interface clock is configurable;
- The effective level of the signals from 8080 or 6800 interface is configurable;
- The interface is driven in the "automatic mode" and the "manual mode". In the "automatic mode", the signals at the ports are driven by LCDI, while the "manual mode" is equivalent to GPIO.
- TX/RX interrupt can be generated, and the interrupt enabling is configurable;

3.1.11 Keyboard control unit (KCU)

The keyboard control unit is used for scanning and identification of the keys on the keyboard, and provided with the security feature of anti-electromagnetic attack. The main characteristics include:

- Provision of up to 4x5 array, and 20 keys;
- Configuration of the debounce time for the keys;
- 4 key cache registers;
- Detection of Push button and Release button;

- Random keyboard scanning against electromagnetic attack;
- Built-in and pull-up of the keyboard array port is the chip IO;
- The pressing-down of multiple keys at the same time is not supported.

3.1.12 DMA controller (DMAC)

Direct memory access (DMA) is used to provide high-speed data transmission between peripherals and memory or between memory and memory. Data can be moved quickly through DMA without CPU intervention, so as to free up CPU resources for other operations.

The DMA controller has eight channels, each of which is specially used to manage the requests for access from memory to memory, from memory to peripheral, and from peripheral to memory. The setting of independent priority is assigned to each channel.

The main characteristics include:

- 8 independent configurable channels
- 8 independent hardware DMA requests (DMA hard handshake interface), each channel also supports software departure (DMA soft handshake interface)
- Independent setting of priority for 8 channels
- Support multi-width data transmission
- Each channel has its own interrupt signal and flag
- Support the transmission from memory to memory, from memory to peripheral, and from peripheral to memory

3.1.13 DCMI interface

The digital camera interface (DCMI) is a synchronous parallel interface capable of receiving high-speed data streams from external 8-, 10-, 12- or 14-bit CMOS camera modules. It supports different data formats: video and compressed data. DCMI interface can receive high speed (up to 54MB/s) data stream. The interface contains up to 14 data lines and a pixel clock line. The polarity of the pixel clock can be programmed so as to capture the data on the rising and falling edges of the pixel clock.

Functional characteristics:

- Support 8-bit, 10-bit, 12-bit, or 14-bit parallel interfaces
- Support synchronization and frame synchronization of embedded code/external line
- Support continuous mode or snapshot mode

- Support clipping function
- Supports 8/10/12/14-bit line-by-line video in the following data formats: Monochrome or raw Bayer format

3.2 Description of CPU resources

3.2.1 MPU

Please refer to the file ARMv7 Protected Memory System Architecture for details.