MEGAHUNT

MH1902T(Ares)
Brief Introduction

Highly Integrated Secure SOC

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Megahunt Tehnologies Inc.

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1 Overview of MH1902T(ARES)

1.1 Description of MH1902T(ARES)

With 32 bit security core processor and the basic frequency up to 144MHz, MH1902T(Ares) makes full use of its excellent architectural characteristics and the high performance so as to achieve the high performance and provide the safe and energy-saving solutions.

With the built-in security encryption module, the chip supports a variety of encryption security algorithms, including DES, TDES, AES, RSA, ECC, SHA, and other encryption algorithms. MH1902T(Ares) also supports a variety of attack detections, and conforms to the financial payment equipment safety standards.

Ares contains the safety BOOT program, supporting the verification of firmware signature upon downloading and starting. In addition to the built-in 128KB SRAM, Ares also integrates abundant peripheral resources, including Smartcard, magnetic stripe card decoding, security keyboard, etc. All the peripheral driver software is compatible with the current mainstream security devices interfaces . The users can develop and transplant quickly on the basis of the existing solutions.

With advanced manufacturing process, Ares can provide higher working frequency and lower power consumption, which are ideal for the design of sorts of smart terminals.

1.2 Main functions and characteristics of MH1902T(Ares)

- 32-bit RISC Core
  - 32-bit RISC Core
  - MPU memory protection unit
  - 144/120/108/72/60/54MHz frequencies（adjustable for 1/2/4 frequency division）
  - 1 controlled JTAG-DP/SW-DP debugging port
- 128KB build-in SRAM
- System control module (To control all peripheral module clocks and system-related configurations)
- Security encryption algorithm accelerator engine
  - Symmetric algorithms：DES、TDES、AES-128/192/256
  - Asymmetric algorithms：RSA-1024/2048、ECC
  - HASH check algorithm：SHA-1/224/256/384/512
- 3 UART interfaces (Supporting 4 lines)
- 1 SmartCard interface (supporting EMV level-1 specification, ISO7816-3 standard), where SCI0 integrates 7816 level conversion function, and can be configured with output of 3V and 1.8V

- 3 SPI interfaces (one can be configured as master or slave, another 2 interfaces support only Master)
- One high-speed SPI interface SPI3(mater/slave configurable)
- One I2C interface
- Six 32-bit TIMER (With PWM function)
- One true random number generator
- One DMA controller (supporting 4-channel DMA transmission)
- One CRC module (Supporting 16Bit/32Bit, a variety of common polynomial calculation)
- Support up to 8 static Tampers or 4 groups of dynamic Tampers (2 outputs, 2 inputs), dynamic/static state configurable
- One group of internal Sensors (Supporting detection of high and low voltage, high and low temperature, Mesh, clock and voltage glitch)
- Secret key storage area (Supporting rapid erase)
- One USB（OTG-FS）
  - USB2.0 and OTG1.0a
  - Built-in USB PHY
  - Dedicated DMA channel and interrupt vector, to speed-up the data communication
- Built-in watchdog
- One 10-bit ADC with 7 channels. supporting up to 1MHz sampling rate. Channel 0 is used for acquisition of voltage ranging from 0~5V(internal bleeder 1.7M/425K) , while other channels are used for acquisition for voltage ranging from 0 ~ 1.2V.
- One 10bit DAC
- Built-in magnetic stripe card decoding module, supporting the standard cards such as ISO/ABA, AAMVA, IBM and JIS II
- Built-in USB charging management module, supporting charging current up to 200 mA
- Built-in the power-on/off function
- Support the output of 27.12M frequency

1.3 Applications of MH1902T(ARES)

Financial security equipments, mobile security terminals, and other smart terminals with sensitive cost and power consumption.

1.4 Basic Description of MH1902T(ARES) structure

MH1902T(Ares) includes 32 bit security core, with 128 KB SRAM, system control module, security encryption module, true random number module, 1 QSPI controller, one 4-channel DMA controller, 1 USB interface, 1 GPIO module, 1 WDT module, 1 BPU module, six 32-bit Timer, 1 CRC module, 3 SPI interfaces, 1 high-speed SPI interface, 1 SCI interface, 3 UART interfaces, 1 DAC, one 7-channel ADC, 1 TRNG module. The block diagram of Ares is shown in Fig 1.1:

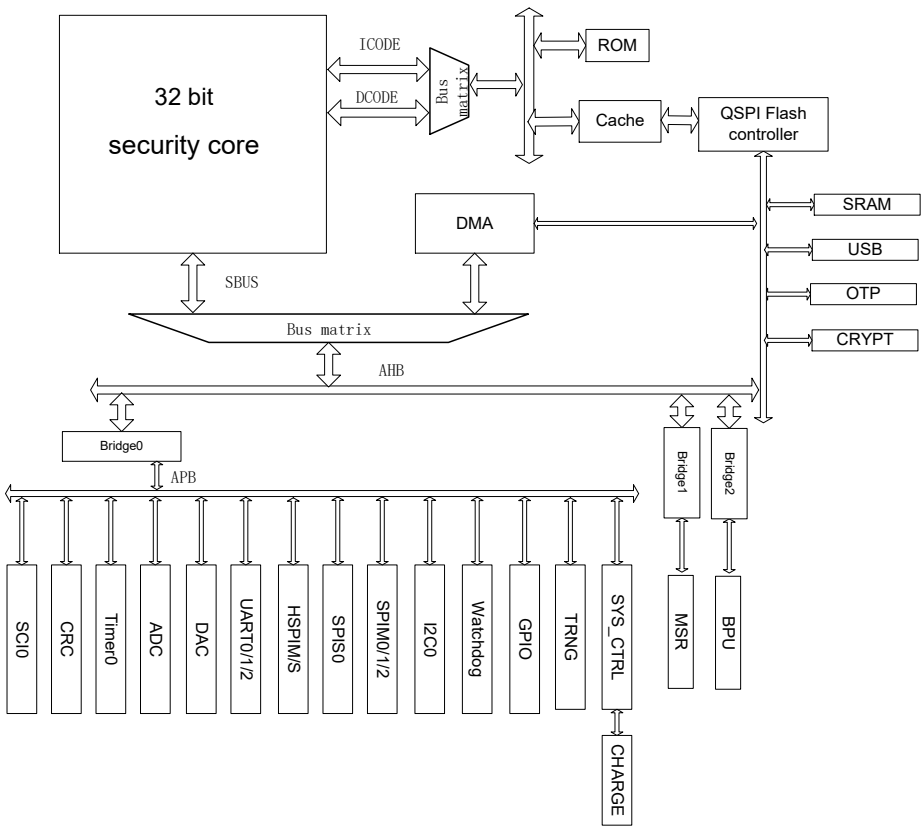


Figure 1- 1Main functional blocks of Ares

2 Characteristics of MH1902T(Ares)

2.1 Electrical characteristics

TABLE 2- 1 Ultimate Parameters

PARAMETERS	DESCRIPTION	RANGE	UNIT
VDD	Operating Voltage	-0.3 to 3.6	V
Iddpd	Power-off current	--	nA
Tamb	Operating temperature	-40~+80	℃
Tstg	Storage temperature	-40~+125	℃
Ground	Ground	-0.3~0.3	V

PARAMETERS	DESCRIPTION	RANGE	UNIT
Voh	Digital output high level	VDD -0.3 ~ VDD+0.3	V
Vol	Digital output low level	<0.4	V
Ioh	Output current	20	mA
Iol	Injected current	20	mA
Vih	Digital input high level	≥0.7×VDD	V
ViL	Digital input low level	≤0.3×VDD	V

TABLE 2- 2 Electrical Characteristics

PARAMETERS	CONDITION（-40°C to +85°C）	VALUE		UNIT
		MIN	MAX	
AVD33		2.7	3.6	V
VDD33		2.7	3.6	V
VBAT33		1.9	3.6	V
CHARGE_VCC		4.6	5.5	V
Vol	VDD=3.3V	-	0.4	V
Voh	VDD=3.3V	VDD – 0.3	-	V
VIH	VDD=3.3V	0.7×VDD	-	V
VIL	VDD=3.3V	-	0.3×VDD	V

TABLE 2- 3 Safety-related Characteristics

SENSOR	DESCRIPTION	RANGE	UNIT
Temperature sensor	High temperature detection	90~120	℃
	Low temperature detection	-30 ~ -50	℃
Voltage sensor	High voltage detection range of operating voltage	4.2±0.1	V
	Low voltage detection range of operating voltage	2.7~2.9	V
	High voltage detection range of battery voltage	4.2±0.1	V
	Low voltage detection range of battery voltage	2.1±0.1	V
Clock/frequency sensor	Detection range of the 12M clock frequency	12±50%	MHz
	Detection range of the 32K clock frequency	32±50%	KHz
External Tamper resistor	Value of pull-up resistors on Tamper pins	3.8M±10%	Ω

TABLE 2- 4 List of Power Consumption

MODE	DESCRIPTION	POWER CONSUMPTION	UNIT
RUN	● All peripherals are turned on ■ @144MHz ● All peripherals are turned off ■ @144MHz	42 22	mA
CPU Sleep	All peripherals are turned off @144MHz	7.2	mA
DeepSleep	● Supporting IO low level、RTC、attacking、charging and card-swiping wake-up	200	uA
PowerDown	● Supporting IO low level、RTC、attacking、charging and card-swiping wake-up	20	uA
VBAT	With all the Tamper pins suspended during the test and the internal pulling resistors are turned on ■ All internal sensors are turned on ■ All internal sensors are turned off	 1.8 1.6	uA

TABLE 2- 5 PARAMETERS OF INTERNAL CHARGING MODULE

Value of programmable resistor	Trickle charging current(mA)	Trickle Threshhold(V)	Constant Charging Current(mA)	Charging Voltage(V)
1K	20±1	2.87±0.01	193±5	4.15±.0.05
2K	10±1	2.88±0.01	96±2	4.15±.0.05
4.02K	5±1	2.90±0.01	46.5±1.5	4.15±.0.05

2.2 PIN DIAGRAM

2.2.1 QFN68

TABLE 2-7 MH1902T(ARES) QFN68 8mm×8mm PIN DEFINITION

PIN No.	PIN name	ALT0	ALT1 (default)	ALT2	ALT3	NOTE
1	PA4		PA[4]	PWM4	XTAL32K	
2	PA5		PA[5]	PWM5	27.12M	Output of 27.12M configurable
3	PA8	SCI0_CLK	PA[8]			In the case of IO multiplexing, the IC card power must be turned on first, and
4	PA9	SCI0_RSTN	PA[9]			
5	PA10	SCI0_IO	PA[10]			

						the high level of the output signal is the IC card output level
6	CVCC					IC card power supply
7	VDD33					
8	POWER_KEY					
9	EN_LDO5V					External LDO Enable
10	**VSS**					GND of Ares
11	PA6	SCI0_DET	PA[6]			
12	PA13		PA[13]	CLK_27P12	UART0_RTS	Output of 27.12M configurable
13	PA15		PA[15]	UART2_TX	UART0_TX	
14	PA0	UART0_RX	PA[0]	PWM0		
15	PA1	UART0_TX	PA[1]	PWM1		
16	PA2	UART0_CTS	PA[2]	PWM2		
17	PA3	UART0_RTS	PA[3]	PWM3		
18	PB0	I2C0_SCL	PB[0]	PWM0	XTAL32K	
19	PB1	I2C0_SDA	PB[1]	PWM1	CLK_27P12	
20	PD4	UART1_RX	PD[4]			
21	PD5	UART1_TX	PD[5]			
22	PB2	SPI0_SCK	PB[2]	PWM2	SPI3_CLK	
23	PB3	SPI0_CSN0	PB[3]	PWM3	SPI3_CSN0	
24	PB4	SPI0_MOSI	PB[4]	PWM4	SPI3_MOSI	
25	PB5	SPI0_MISO	PB[5]	PWM5	SPI3_MISO	
26	VDD33					IO Supply
27	PB12	SPI2_CLK	PB[12]	SPI3_CLK	UART1_RX	
28	PB13	SPI2_CSN	PB[13]	SPI3_CSN0	UART1_TX	
29	PB14	SPI2_MOSI	PB[14]	SPI3_MOSI	UART1_CTS	
30	PB15	SPI2_MISO	PB[15]	SPI3_MISO	UART1_RTS	
31	VDD12					Connect 1uF capacitor
32	RST_N					
33	PC9	UART2_CTS	PC[9]		SPI1_MOSI	
34	PC10	UART2_RX	PC[10]		SPI1_CLK	
35	PC15	SPI1_MISO	PC[15]	SPI3_MISO	UART2_TX	
36	PC14	SPI1_MOSI	PC[14]	SPI3_MOSI	UART2_RTS	
37	PC13	SPI1_CLK	PC[13]	SPI3_CLK	UART2_RX	
38	PC12	SPI1_CSN	PC[12]	SPI3_CSN	UART2_CTS	
39	CHARGE_VPROG					CHARGE current Control Pin
40	CHARGE_VCC					CHARGE Supply Input

41	CHARGE_VBAT					CHARGE Supply Output, connect battery
42	MSR_IN1	UART1_CTS	PD[6]	MSR_IN1	I2C0_SCL	Magnetic strip card T1+
43	MSR_IN2	UART1_RTS	PD[7]	MSR_IN2	I2C0_SDA	Magnetic strip card T1-
44	MSR_IN3	SPI1_SCK	PD[8]	MSR_IN3		Magnetic strip card T2+
45	MSR_IN4	SPI1_CSN	PD[9]	MSR_IN4		Magnetic strip card T2-
46	MSR_IN5	SPI1_MOSI	PD[10]	MSR_IN5		Magnetic strip card T3+
47	MSR_IN6	SPI1_MISO	PD[11]	MSR_IN6		Magnetic strip card T3-
48	PC5		PC[5]	ADC_IN5		
49	PC4	TCK	PC[4]	ADC_IN4		
50	PC3	TMS	PC[3]	ADC_IN3	UART1_RTS	
51	PC2	TDO	PC[2]	ADC_IN2	UART1_CTS	
52	PC1	TDI	PC[1]	ADC_IN1/DAC	UART1_TX	
53	PC0	TRST	PC[0]	ADC_IN0	UART1_RX	
54	DN					USB DN
55	DP					USB DP
56	VBUS					USB VBUS
57	ID					USB ID
58	XI12M					XTAL 12MHz Input
59	XO12M					XTAL12MHz Output
60	VDD33					IO Supply
61	AVD33					Analog Supply
62	XO32					XTAL 32KHz Output
63	XI32					XTAL 32KHz Input
64	EXTS3					External Tamper3
65	EXTS1					External Tamper1
66	EXTS2					External Tamper2
67	EXTS0					External Tamper0
68	VBAT33					Battery-powered supply

2.2.2 QFN88

TABLE 2-8 MH1902T(ARES) QFN88 10mm×10mm PIN DEFINITION

PIN No.	PIN name	ALT0	ALT1 (default)	ALT2	ALT3	NOTE
1	PA4		PA[4]	PWM4	XTAL32K	
2	PA5		PA[5]	PWM5	CLK_27P12	Output of 27.12M configurable
3	PA8	SCI0_CLK	PA[8]			In the case of IO multiplexing, the IC card power must be turned on first, and the high level of the output signal is the IC card output level
4	PA9	SCI0_RSTN	PA[9]			
5	PA10	SCI0_IO	PA[10]			
6	CVCC					IC card power supply
7	VDD33					
8	POWER_KEY					
9	EN_LDO5V					External LDO Enable
10	**VSS**					GND of Ares
11	PA6	SCI0_DET	PA[6]			
12	PA7		PA[7]	CLK_27P12		Output of 27.12M configurable
13	PA11		PA[11]			
14	PA12		PA[12]		UART0_CTS	
15	PA13		PA[13]	CLK_27P12	UART0_RTS	Output of 27.12M configurable
16	PA14	SCI0_VCCEN	PA[14]	UART2_RX	UART0_RX	
17	PA15		PA[15]	UART2_TX	UART0_TX	
18	PA0	UART0_RX	PA[0]	PWM0		UART download pin
19	PA1	UART0_TX	PA[1]	PWM1		
20	PA2	UART0_CTS	PA[2]	PWM2		
21	PA3	UART0_RTS	PA[3]	PWM3		
22	PB0	I2C0_SCL	PB[0]	PWM0	XTAL32K	
23	PB1	I2C0_SDA	PB[1]	PWM1	CLK_27P12	
24	PD4	UART1_RX	PD[4]			
25	PD5	UART1_TX	PD[5]			
26	PB2	SPI0_SCK	PB[2]	PWM2	SPI3_CLK	
27	PB3	SPI0_CSN0	PB[3]	PWM3	SPI3_CSN0	
28	PB4	SPI0_MOSI	PB[4]	PWM4	SPI3_MOSI	
29	PB5	SPI0_MISO	PB[5]	PWM5	SPI3_MISO	

30	IO_VCC					PB2~PB5 Supply Input
31	PB12	SPI2_CLK	PB[12]	SPI3_CLK	UART1_RX	
32	PB13	SPI2_CSN	PB[13]	SPI3_CSN0	UART1_TX	
33	PB14	SPI2_MOSI	PB[14]	SPI3_MOSI	UART1_CTS	
34	PB15	SPI2_MISO	PB[15]	SPI3_MISO	UART1_RTS	
35	PB10		PB[10]			
36	PB11		PB[11]			
37	PC6		PC[6]		CLK_27P12	
38	PC7		PC[7]			
39	PC8	UART2_TX	PC[8]		SPI1_MISO	
40	VDD12					Connect 1uF capacitor
41	RST_N					
42	PC9	UART2_CTS	PC[9]		SPI1_MOSI	
43	PC10	UART2_RX	PC[10]		SPI1_SCK	
44	PB6	SPI1_SCK	PB[6]	SPI3_SCK		
45	PB7	SPI1_CSN0	PB[7]	SPI3_CSN0		
46	PB8	SPI1_MOSI	PB[8]	SPI3_MOSI		
47	PB9	SPI1_MISO	PB[9]	SPI3_MISO		
48	PC15	SPI1_MISO	PC[15]	SPI3_MISO	UART2_TX	
49	PC14	SPI1_MOSI	PC[14]	SPI3_MOSI	UART2_RTS	
50	PC13	SPI1_CLK	PC[13]	SPI3_CLK	UART2_RX	
51	PC12	SPI1_CSN	PC[12]	SPI3_CSN	UART2_CTS	
52	PC11	UART2_RTS	PC[11]		SPI1_CSN0	
53	CHARGE_VPROG					CHARGE current Control Pin
54	CHARGE_VCC					CHARGE Supply Input
55	CHARGE_VBAT					CHARGE Supply Output
56	PD6	UART1_CTS	PD[6]	MSR_IN1	I2C0_SCL	Magnetic strip card T1+
57	PD7	UART1_RTS	PD[7]	MSR_IN2	I2C0_SDA	Magnetic strip card T1-
58	PD8	SPI1_SCK	PD[8]	MSR_IN3		Magnetic strip card T2+
59	PD9	SPI1_CSN	PD[9]	MSR_IN4		Magnetic strip card T2-
60	PD10	SPI1_MOSI	PD[10]	MSR_IN5		Magnetic strip card T3+
61	PD11	SPI1_MISO	PD[11]	MSR_IN6		Magnetic strip card T3-
62	PC5		PC[5]	ADC_IN5		
63	PC4	TCK	PC[4]	ADC_IN4		
64	PC3	TMS	PC[3]	ADC_IN3	UART1_RTS	
65	PC2	TDO	PC[2]	ADC_IN2	UART1_CTS	

66	PC1	TDI	PC[1]	ADC_IN1/DAC	UART1_TX	
67	PC0	TRST	PC[0]	ADC_IN0	UART1_RX	
68	VDD33					IO Supply
69	PD0	DRV_VBUS	PD[0]			
70	**VSS**					GND of Ares
71	DN					USB DN
72	DP					USB DP
73	VBUS					USB VBUS
74	ID					USB ID
75	XI12M					XTAL 12MHz Input
76	XO12M					XTAL12MHz Output
77	VDD33					
78	EXTS7					External Tamper7
79	EXTS5					External Tamper5
80	XO32					XTAL 32KHz Output
81	XI32					XTAL 32KHz Input
82	EXTS6					External Tamper6
83	EXTS4					External Tamper4
84	EXTS3					External Tamper3
85	EXTS1					External Tamper1
86	EXTS2					External Tamper2
87	EXTS0					External Tamper0
88	VBAT33					Battery-powered supply

2.2.3 BGA121

TABLE 2- 9 MH1902T(ARES) BGA121 8mm×8mmPIN DEFINITION

PIN No.	PIN name	ALT0	ALT1 (default)	ALT2	ALT3	NOTE
A1	PA8	SCI0_CLK	PA[8]			In the case of IO multiplexing, the IC card power must be turned on first, and the high level of the output signal is the IC card output level
A2	XI32					XTAL 32KHz Input
A3	XO32					XTAL 32KHz Output
A4	PA4		PA[4]	PWM4	XTAL32K	

A5	PA5		PA[5]	PWM5	CLK_27P12	Output of 27.12M configurable
A6	XO12M					XTAL12MHz Output
A7	XI12M					XTAL 12MHz Input
A8	ID					USB ID
A9	VBUS					USB VBUS
A10	DP					USB DP
A11	DN					USB DN
B1	PA9	SCI0_RSTN	PA[9]			In the case of IO multiplexing, the IC card power must be turned on first, and the high level of the output signal is the IC card output level
B2	PA10	SCI0_IO	PA[10]			
B3	PA6	SCI0_DET	PA[6]			
B4	NC					
B5	**VSS**					
B6	NC					
B7	NC					
B8	NC					
B9	PC0	TRST	PC[0]	ADC_IN0	UART1_RX	
B10	PC1	TDI	PC[1]	ADC_IN1/DAC	UART1_TX	
B11	PD0	DRV_VBUS	PD[0]			
C1	NC					
C2	NC					
C3	NC					
C4	CVCC					IC card supply
C5	VBAT33					Battery-powered supply
C6	NC					
C7	VDD33					
C8	NC					
C9	PC2	TDO	PC[2]	ADC_IN2	UART1_CTS	
C10	PC3	TMS	PC[3]	ADC_IN3	UART1_RTS	
C11	PC4	TCK	PC[4]	ADC_IN4		
D1	PA11		PA[11]			
D2	PC14	SPI1_MOSI	PC[14]	SPI3_MOSI	UART2_RTS	
D3	PC15	SPI1_MISO	PC[15]	SPI3_MISO	UART2_TX	
D4	PC5		PC[5]	ADC_IN5		
D5	NC					

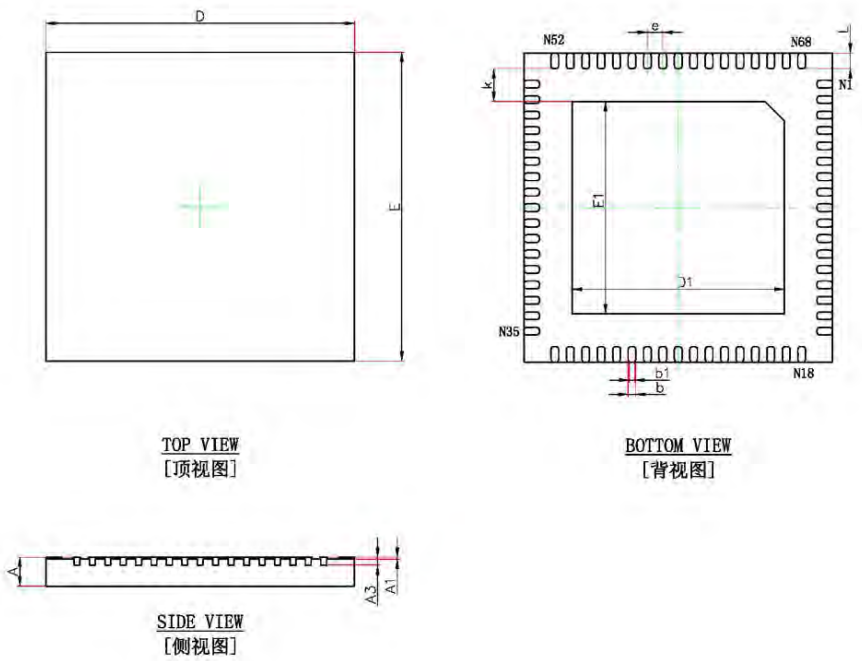
D6	PA14		PA[14]	UART2_RX	UART0_RX	
D7	PA13		PA[13]		UART0_RTS	
D8	PA12		PA[12]		UART0_CTS	
D9	PD10	SPI1_MOSI	PD[10]	MSR_IN5		Magnetic strip card T3+
D10	PD11	SPI1_MISO	PD[11]	MSR_IN6		Magnetic strip card T3-
D11	NC					
E1	NC					
E2	**VSS**					
E3	VDD33					
E4	NC					
E5	EXTS2					External Tamper2
E6	EXTS5					External Tamper5
E7	PA15		PA[15]	UART2_TX	UART0_TX	
E8	**VSS**					
E9	PD8	SPI1_SCK	PD[8]	MSR_IN3		Magnetic strip card T2+
E10	PD9	SPI1_CSN	PD[9]	MSR_IN4		Magnetic strip card T2-
E11	CHARGE_VBAT					CHARGE Supply Output
F1	PD4	UART1_RX	PD[4]			
F2	PD5	UART1_TX	PD[5]			
F3	NC					
F4	NC					
F5	EXTS1					External Tamper1
F6	EXTS4					External Tamper4
F7	EXTS7					External Tamper7
F8	NC					
F9	PD6	UART1_CTS	PD[6]	MSR_IN1	I2C0_SCL	Magnetic strip card T1+
F10	PD7	UART1_RTS	PD[7]	MSR_IN2	I2C0_SDA	Magnetic strip card T1-
F11	CHARGE_VCC					CHARGE supply input
G1	PA0	UART0_RX	PA[0]	PWM0		UART download pin
G2	PA1	UART0_TX	PA[1]	PWM1		
G3	PA2	UART0_CTS	PA[2]	PWM2		
G4	PA3	UART0_RTS	PA[3]	PWM3		
G5	EXTS0					External Tamper0
G6	EXTS3					External Tamper3
G7	EXTS6					External Tamper6
G8	NC					
G9	NC					
G10	PC7		PC[7]			

G11	CHARGE_VPROG					CHARGE current control pin
H1	PB6	SPI1_SCK	PB[6]	SPI3_SCK		
H2	PB7	SPI1_CSN0	PB[7]	SPI3_CSN0		
H3	PB3	SPI0_CSN0	PB[3]	PWM3	SPI3_CSN0	
H4	IO_VCC					PB2~PB5 supply input
H5	NC					
H6	NC					
H7	VDD33					
H8	PC8	UART2_TX	PC[8]		SPI1_MISO	
H9	PC10	UART2_RX	PC[10]		SPI1_SCK	
H10	PC12	SPI1_CSN	PC[12]	SPI3_CSN	UART2_CTS	
H11	PC13	SPI1_CLK	PC[13]	SPI3_CLK	UART2_RX	
J1	NC					
J2	**VSS**					
J3	PB4	SPI0_MOSI	PB[4]	PWM4	SPI3_MOSI	
J4	NC					
J5	NC					
J6	**VSS**					
J7	NC					
J8	PB10		PB[10]			
J9	PB11		PB[11]			
J10	PC11	UART2_RTS	PC[11]		SPI1_CSN0	
J11	PC9	UART2_CTS	PC[9]		SPI1_MOSI	
K1	PB1	I2C0_SDA	PB[1]	PWM1	CLK_27P12	
K2	PC6		PC[6]		CLK_27P12	
K3	NC					
K4	NC					
K5	NC					
K6	PB13	SPI2_CSN	PB[13]	SPI3_CSN0	UART1_TX	
K7	PB15	SPI2_MISO	PB[15]	SPI3_MISO	UART1_RTS	
K8	NC					
K9	RST_N					
K10	PB8	SPI1_MOSI	PB[8]	SPI3_MOSI		
K11	PB9	SPI1_MISO	PB[9]	SPI3_MISO		
L1	PB0	I2C0_SCL	PB[0]	PWM0	XTAL32K	
L2	PB2	SPI0_SCK	PB[2]	PWM2	SPI3_CLK	
L3	PB5	SPI0_MISO	PB[5]	PWM5	SPI3_MISO	
L4	NC					
L5	NC					
L6	PB12	SPI2_CLK	PB[12]	SPI3_CLK	UART1_RX	
L7	PB14	SPI2_MOSI	PB[14]	SPI3_MOSI	UART1_CTS	

L8	PA7		PA[7]			
L9	VDD12					Connect 1uF capacitor
L10	NC					
L11	NC					

2.3 PACKAGE INFORMATION

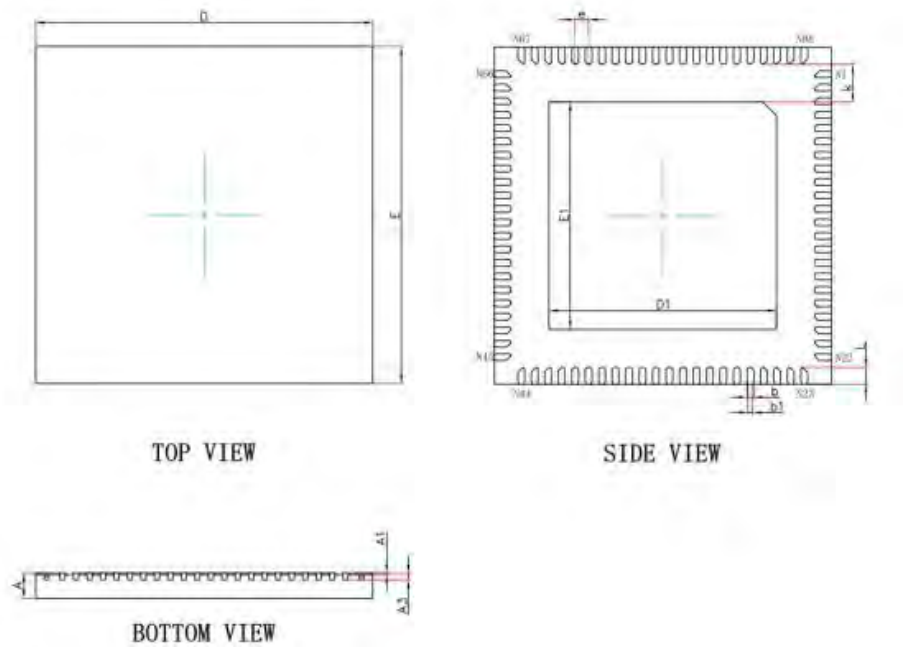
2.3.1 QFN68



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	7.900	8.100	0.311	0.319
E	7.900	8.100	0.311	0.319
D1	5.400	5.600	0.213	0.220
E1	5.400	5.600	0.213	0.220
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
b1	0.100	0.200	0.004	0.008
e	0.400TYP.		0.016TYP.	
L	0.324	0.476	0.013	0.019

FIGURE 2- 1 MH1902T(ARES) QFN68 8mm*8mm PACKAGE SIZE

2.3.2 QFN88



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	9.900	10.100	0.390	0.398
E	9.900	10.100	0.390	0.398
D1	6.650	6.850	0.262	0.270
E1	6.650	6.850	0.262	0.270
k	1.125REF.		0.044REF.	
b	0.150	0.250	0.006	0.010
b1	0.150REF.		0.006REF.	
e	0.400BSC.		0.016BSC.	
L	0.400	0.600	0.016	0.024

FIGURE 2- 2 MH1902T(ARES) QFN88 10mm*10mm PACKAGE SIZE

2.3.3 BGA121

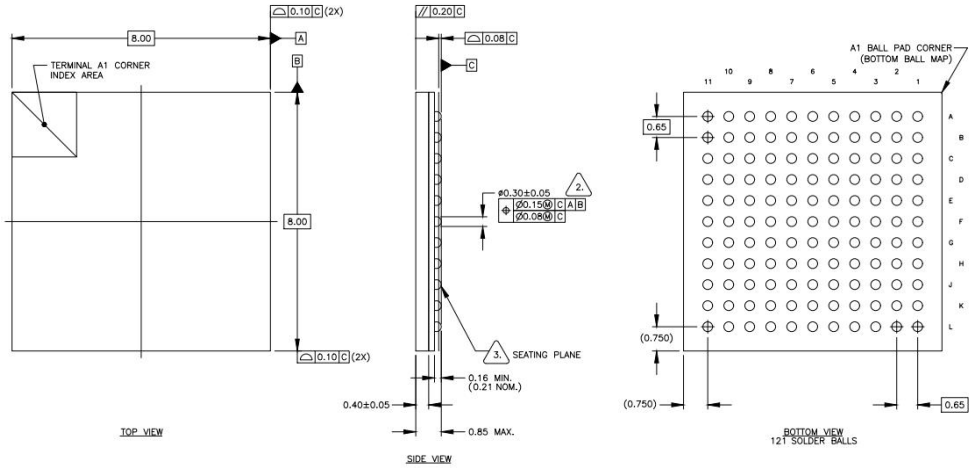


FIGURE 2- 3 MH1902T(ARES) BGA121 8mm*8mm PACKAGE SIZE

2.4 ORDERING INFORMATION

TABLE 2- 10 MH1902T(ARES) ORDERING INFORMATION

BASIC PARAMETER / PART NUMBER	SRAM	Flash	Scan Algorithm	Package
MH1902TQ67MH0S	128KB	1MB	General Version	QFN68
MH1902TQ87NH0S	128KB	4MB	General Version	QFN88
MH1902TBB7NH00	128KB	4MB	--	BGA121
(void)				

3 Description of Functional Modules

3.1 Peripherals

3.1.1 SPI

Ares provides one SPI master/slave and two SPI master interfaces. The SPI master interface can support communication with multiple slave devices.

Characteristics of SPI peripherals ：

- Operation of Master mode and Slave mode at independent addresses
- Master mode supports full duplex, simplex receiving, simplex transmitting, EEPROM mode
- Multiple Master conflict detection
- Support three communication modes including Motorola SPI, Texas Instruments SPI, and National Semiconductor Microwire
- Receive and transmit FIFO independently at the depth of 16 and the fixed width of 16 bits
- The frame length is configurable, ranging from 4 to 16 bits
- DMA interface

The common Motorola SPI communication protocol supports four communication modes, so as to achieve full duplex communication. The default mode 0 is used to power on the system.

The 4 communication modes as specified in SPI protocol are described as follows:

- Mode 0: Clock polarity (CPOL) = 0, clock phase (CPHA) = 0. In this mode, the idle state of the serial synchronous clock is low level, and the chip will take sample at the first jump edge (rising edge) of the serial synchronous clock. The chip defaults to this mode.
- Mode 1: Clock polarity (CPOL) = 0, clock phase (CPHA) = 1. In this mode, the idle state of the serial synchronous clock is low level, and the chip will take sample at the second jump edge (falling edge) of the serial synchronous clock.
- Mode 2: Clock polarity (CPOL) = 1, clock phase (CPHA) = 0. In this mode, the idle state of the serial synchronous clock is high level, and the chip will take sample at the first jump edge (rising edge) of the serial synchronous clock.
- Mode 3: Clock polarity (CPOL) = 1, clock phase (CPHA) = 1. In this mode, the idle state of the serial synchronous clock is high level, and the chip will take sample at the second jump edge (rising edge) of the serial synchronous clock.

Note: In order to ensure the normal operation of the SPI, keep the CSN signal

line at the high level during the process of mode switching. At the same time, if the master thinks that there is an error in the slave during the process of communication, the slave can return to normal by raising the CSN.

SPI interfaces are described as follows:

- SCK: The clock input pin of SPI; when the communication rate of 200K is adopted, the delay of 20us is needed between the bytes as a minimum;
- CSN: The chip selection signal of SPI, which is the input pin of the chip, with low efficiency;
- MOSI: The data input pin of SPI;
- MISO: The data output pin of SPI.

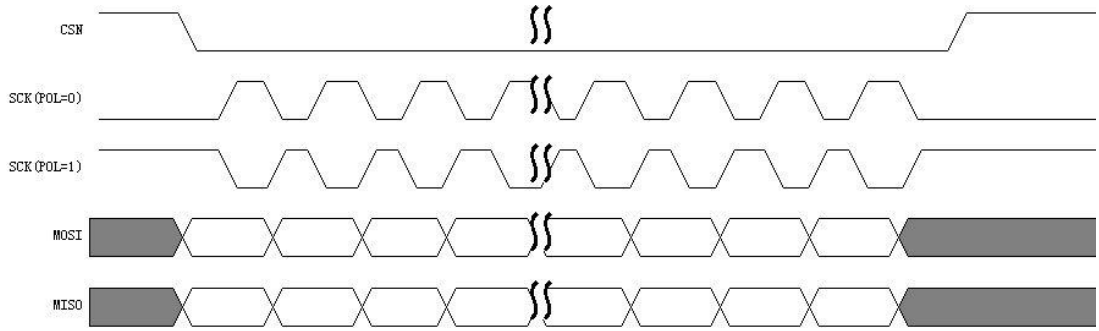


Figure 3 SPI Time Sequence 1 (CPHA=0)

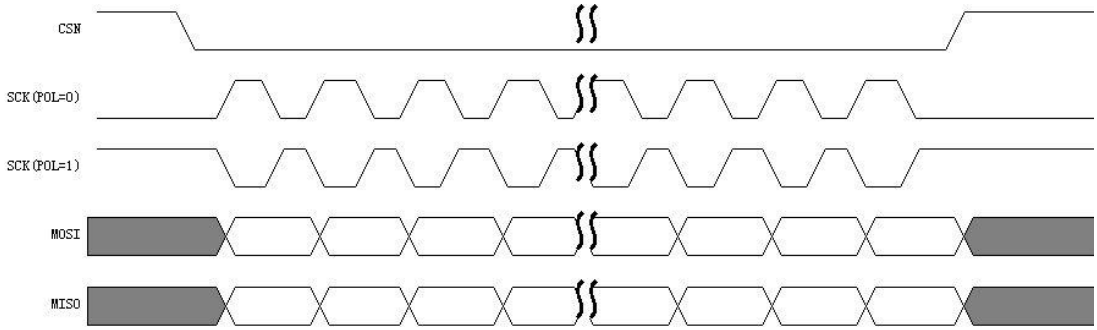


Figure 4 SPI Time Sequence 2 (CPHA=1)

3.1.2 High-speed SPI

Ares provides one high-speed SPI master interface, supporting the communication with multiple slave devices.

Characteristics of HSPI peripherals:

- The Master mode supports the full duplex mode
- Receive and transmit FIFOs are independent, and the interrupt

threshold for receiving and transmitting FIFO is configurable

- Receive and transmit FIFO at the depth of 64
- DMA interface

The common Motorola SPI communication protocol supports four communication modes, so as to achieve the full duplex communication. The default mode 0 is used to power on the system.

3.1.3 UART

Ares has three full-duplex UART serial interfaces, all of which support 4-wire mode.

Characteristics of UART peripherals:

- Receive and transmit FIFO independently at the depth of 16 bytes
- Control of FIFO enabling
- Setting of data bits, supporting 5-8bit
- Forced output of 9 check bits
- Frame error, check error, break interrupt detection
- IrDA 1.0 protocol support
- DMA receiving

UART supports independent receiving and transmitting of FIFO, and FIFO function can be configured for use by enabling bits.

The receiving and transmitting of FIFO by UART supports the full interrupt in receiving FIFO and the empty interrupt in transmitting FIFO respectively, and the trigger values thereof are configurable. The interrupt source in transmitting FIFO shares the same interrupt source with the transmitter holding register empty (THRE) in the non-FIFO mode, which is set by the software.

3.1.4 SCI

Ares has one smart card interface, supporting ISO7816-3 standard and EMV Level-1 specification.

- Support the asynchronous T=0 and T=1 transmission protocols
- The timing sequence and the time parameters of the protocol are configurable
- Receiving and transmitting buffer at depth of 8 characters
- Receiving and transmitting FIFO monitor interrupt
- Interrupt status register
- When the smart card is detected to be removed away, Ares is automatically triggered to activate the timing sequence

- The deactivation timing sequence configurable by software
- Limited support for synchronization cards (control of input and output by register)

The external clock provided by SCI module F = PCLK/2 (SCICLKICC + 1), SCICLKICC bit width is 8bit, ranging from 0 to 255.

3.1.5 USB

OTG_FS controller interface, conforming to USB 2.0 standard and OTG 1.0a specification

- Support USB2.0
- Support OTG1.0a
  - Identify the inserted A-B type devices (ID)
  - Support the host negotiation protocol (HNP) and the session request protocol (SRP)
  - In OTG application, the host is allowed to shut down VBUS to save the power consumption
- Support USB full-speed/low-speed devices (type-B devices) under SRP protocol
  - Support USB full-speed/low-speed devices (type-A devices) under SRP protocol
  - USB OTG full-speed/low-speed dual-role device
- Provide 512-byte private RAM and advanced FIFO management
  - RAM Configure different RAM areas for different FIFOs by the software, so as to make flexible and effective use of RAM
  - Each FIFO can store multiple packets
  - The dynamic allocation of storage areas is allowed
  - The length of FIFO is not limited (The length with a power of 2 is not forced, and the memory area can be used continuously)
  - The same endpoint number is allowed (IN/OUT endpoints share the same FIFO for more efficient use of the memory area)
- The maximum data flow of one frame (1ms) can be guaranteed without system intervention
- With a private DMA channel and the proprietary interrupt vector, the data communication can be accelerated
- Host mode
  - Supports up to four host channels, each of which can be dynamically configured for any type of transmission
  - Support up to four interrupt and synchronous transmission requests in the periodic hardware transmission request queue

- Support up to four transmission requests for control and high capacity transmission in the non-periodic hardware transmission request queue

3.1.6 BPU & Sensor

The built-in BPU module provides BPK unit, Sensor unit and RTC unit.

The BPK unit is powered by the onboard button battery , thus in the case of the failure of the external power supply won't lead to the loss of the data stored in the BPK unit. When the Sensor unit detects an attack, the BPK shall be cleared by the BPK register settled.

Characteristics of sensor:

- Programmable sensors for detection of external attack, support external static and external dynamic mode; in external static mode, up to 8 detection sources can be programmed; in external dynamic mode, up to 4 pairs of detection sources can be programmed.
- Internal attack detection includes 32KHz clock frequency detection, high and low temperature attack detection, and high and low voltage attack detection.
- Active shielding。
- Battery voltage glitch detection.

3.1.7 GPIO

Ares' GPIO pins can be configured by software as output, input, or as peripheral alternate function. All GPIOs can be configured as strong push-pull/open-drain output modes

3.1.8 True random number generator (RNG)

Ares embed a true random number generator(RNG) that provides full entropy outputs to the application as 128-bit samples.