MEGAHUNT

MH1611
Brief Introduction

Highly Integrated Reader/Writer IC for NFC

Version: 1.1
Date: 2020-02-04

Megahunt Tehnologies Inc.

Revision Record

Date	Revised version	Description	Author
2020-1-4	V1.0	First version completed	Megahunt
2020-2-4	V1.1	Isolation between power and ground	Megahunt

Table of Contents

Overview

MH1611 is a highly integrated NFC & EMVCo reader/writer IC. It works at 13.56MHz and supports contactless reader/writer mode complying with ISO/IEC 14443 Type A/B, Felica, ISO/IEC 15693 protocol.

Features

- Wide operating range: 1.8V-6V
- Compliant with EMV3.1 certification
- Effective communication distance up to 10 cm
- Support P2P passive initiator mode of ISO/IEC 18092
- Support Felica card 212K and 424K protocol
- Support ISO/IEC 15693 protocol
- Support communication of ISO 14443 A with high transmission rate: 106kbit/s、212kbit/s、424kbit/s、848kbit/s
- Support MFIN/MFOUT
- Supported host interface:

  －10Mbit/s SPI interface

  －I2C interface, with the rate of 100kbit/s under standard mode

  －Serial UART, transmission rate up to 1228.8kbit/s
- 64 bytes transmitting and receiving FIFO buffer zone
- Flexible interruption mode
- Programmable timer
- With three power-saving modes: hardware power-down, software power-down and transmitter power-down
- With built-in temperature sensor, facilitating the automatic stop of RF emission in case of

excessive high IC core temperature

- Several independent groups of power supplies to avoid the mutual interference between IC internal blocks and improve the stability of the work
- With CRC and parity check function, built-in CRC co-processor, which complies with ISO/1EC14443 and CCITT protocol
- Internal oscillator, connected to 27.12MHz crystal
- Programmable I/O pins
- Support Low Power Card Detection (LPCD)

Operating Conditions

Symbol	Parameters	Condition	Min	Typ	Max	Unit
DVDD	Digital power voltage	VSS=TVSS=AVSS=GND = 0V DVDD<=SVDD<=AVDD <=TVDD	1.8	3.3	6	V
AVDD	Analog power voltage		1.8	3.3	6	V
SVDD	Analog power voltage					
TVDD	Transmitter power voltage					
TA	Working temperature		-40		+85	℃

[1] SVDD and DVDD must be less than or equal to AVDD and TVDD

[2] AVDD must be less than or equal to TVDD

[3] Recommended power supply conditions: SVDD=DVDD=AVDD<=TVDD

Electrical Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
3.3V electrical characteristics						
I_{HPD}	Hard power-down current	AVDD=DVDD=TVDD=PVDD = 3.3V NRSTPD=LOW	—	0.02	—	uA
I_{SPD}	Soft power-off current	AVDD=DVDD=TVDD=PVDD = 3.3V Opening of RF level detector	—	0.7	—	uA
I_{IDLE}	Idle current	AVDD=DVDD=TVDD=PVDD = 3.3V	—	1.5	—	mA
I_{DVDD}	Digital power current	DVDD=3.3V	—	1.2	—	mA
I_{AVDD}	Analog power current	AVDD=3.3V, in case of RCVOff =0	—	3.3	—	mA
	Analog power current	AVDD=3.3V, in case of RCVOff =1	—	3.49	—	mA
I_{TVDD}	Transmitter power current	Continuously transmit carrier, TVDD=3.3V	—	100	170	mA
V_{Ripple}	Power ripple resistance				400	mV
V_{Noise}	Anti-power random noise				1600	mV
R_{TX}	TX1/TX2 output resistance			25		Ω
V_{RX}	RX input sensitivity	fSUB=848kHz		0.5		mVrms
R_{Rx}	Rx input resistance			50		KΩ
V_{POR}	Power-on resetting voltage			1.5		V
T_{OSU}	Starting time of crystal oscillator			300		us

5V electrical characteristics						
I_{HPD}	Hard power-down current	AVDD=DVDD=TVDD=PVDD = 5V	—	0.02	—	uA
		NRSTPD=LOW				
I_{SPD}	Soft power-off current	AVDD=DVDD=TVDD=PVDD = 5V Opening of RF level detector	—	0.9	—	uA
I_{IDLE}	Idle current	AVDD=DVDD=TVDD=PVDD = 5V	—	1.4	—	mA
I_{DVDD}	Digital power current	DVDD=5V	—	1.37	—	mA
I_{AVDD}	Analog power current	AVDD=5V, in case of RCVOff= 0	—	3.5	—	mA
	Analog power current	AVDD=5V, in case of RCVOff= 1	—	3.7	—	mA
I_{TVDD}	Transmitter power current	Continuous emission of carrier, TVDD=5V	—	230	300	mA
V_{Ripple}	Power ripple resistance				300	mV
V_{Noise}	Anti-power random noise				1600	mV
R_{TX}	TX1/TX2 output resistance			20		Ω
V_{RX}	RX input sensitivity	fSUB=848kHz		0.5		mVrms
R_{Rx}	Rx input resistance			50		KΩ
V_{POR}	Power-on resetting voltage			1.5		V
T_{OSU}	Starting time of crystal oscillator			300		us

Examples of working currents:

Card type	Height of card swiping vs. Working current						
	1 cm	2 cm	3 cm	4 cm	5 cm	6 cm	7 cm
S50	10 mA	10 mA	12 mA	15 mA	17 mA	21 mA	25 mA
S70	10 mA	10 mA	12 mA	15 mA	17 mA	21 mA	25 mA
Ultra Light	12 mA	12 mA	14 mA	15 mA	21 mA	25 mA	27 mA

Note:

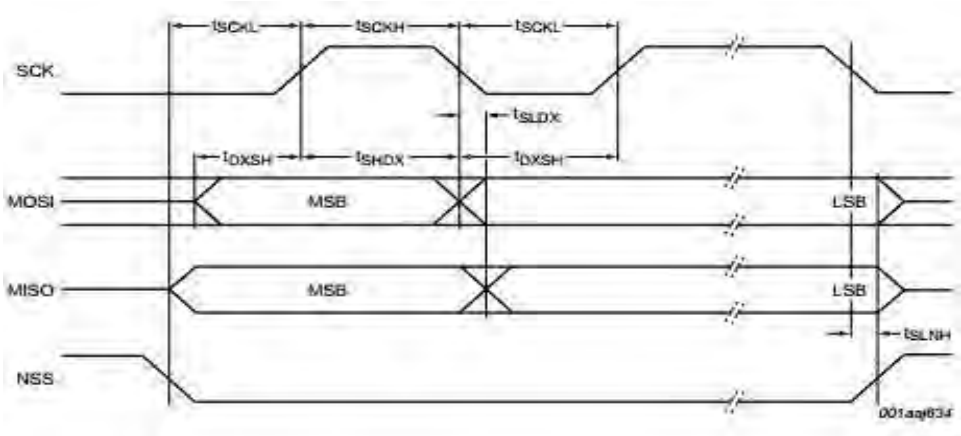
[1] The specific distance of card swiping is influenced by the antenna size and tuning;

[2] Under the same distance, the working current varies due to the different inductive impedance of different type of cards.

SPI Timing Characteristics

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
tSCKL	pulse width LOW	line SCK	50	-	-	ns
tSCKH	pulse width HIGH	line SCK	50	-	-	ns
tSHDX	SCK HIGH to data input hold time	SCK to changing MOSI	25	-	-	ns
tDXSH	data input to SCK HIGH set-up time	changing MOSI to SCK	25	-	-	ns
tSLDX	SCK LOW to data output hold time	SCK to changing MISO	-	-	25	ns
tSLNH	SCK LOW to NSS HIGH time		25	-	-	ns
tNHNL	NSS HIGH time	before communication	50	-	-	ns
t_{DOD}	Data out delay			20		ns
tDOHZ	Data out to high impedance delay			20		ns

SPI Timing Diagram



Note:

[1] The signal NSS must be LOW to be able to send several bytes in one data stream.

[2] To send more than one data stream NSS must be set HIGH between the data streams.

IO Electrical Characteristics

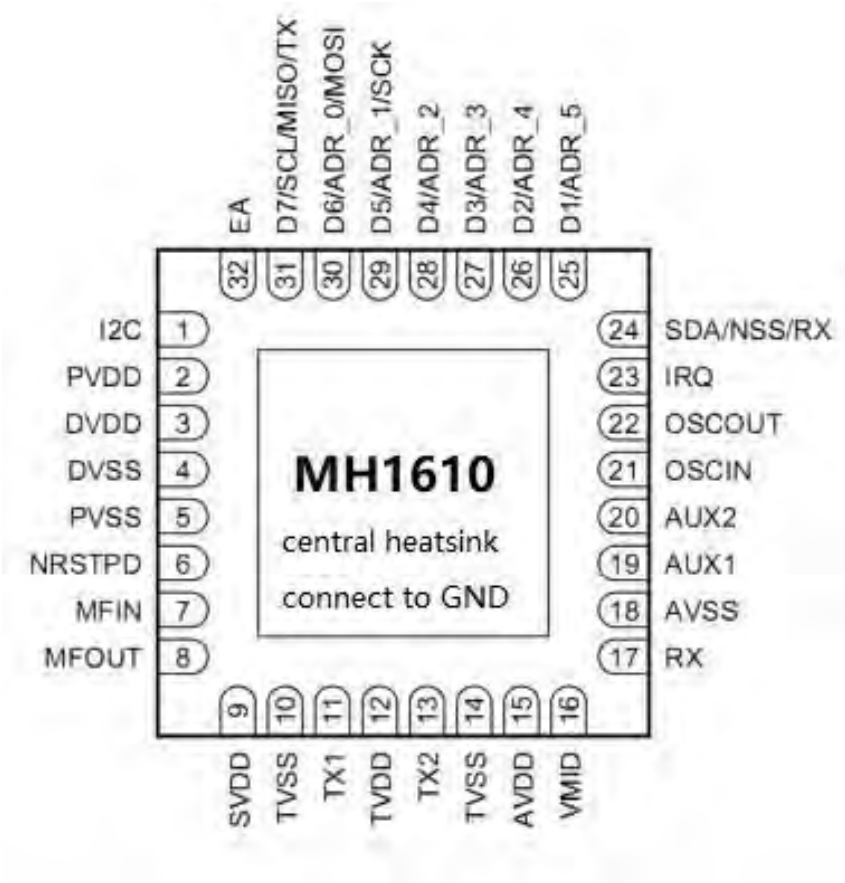
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
EA, I2C, EN						
I_{LEAK}	Input leak current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7P VDD			V
V_{IL}	Input voltage low level				0.3PV DD	V
MFIN						
I_{LEAK}	Input leak current	Under working/sleeping mode, connected with VDD	-1	-	1	uA
		Under working/sleeping mode, connected with GND		14.1		uA
		Under working/sleeping mode, connected with 1.5V		13.1		uA

		Under working/sleeping mode, unconnected		0		uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
NSS						
ILEAK	Input leak current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
OSCIN						
ILEAK	Input leak current	Under working mode, connected with VDD		1.1		uA
		Under working mode, connected with GND		0.6		uA
		Under working mode, connected with 1.5V		0.4		uA
		Under working mode,unconnected	-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
D1, D2, D3, D4						
I_{LEAK}	Input leak current	Under working/sleeping mode, connected with VDD	-1	-	1	uA
		Under working/sleeping mode, connected with GND		13.5		uA
		Under working/sleeping mode, connected with 1.5V		13		uA
		Under working/sleeping mode, unconnected		0		uA
V_{IH}	Input voltage		0.7PVDD			V
	high level					
V_{IL}	Input voltage low level				0.3PVDD	V

V_{OH}	Output voltage high level	VDD(PVDD)=3V; IO=4mA	VDD(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	VDD(PVDD)=3V; IO=4mA	VSS(PVSS)	-	V_{SS}(PVSS)+0.4	V
I_{OH}	High level output current	VDD(PVDD) = 3 V	-8.5		-7.3	mA
I_{OL}	Low level output current	VDD(PVDD) = 3 V	7.3		8.5	mA
SCK, SDI						
I_{LEAK}	Input leak current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
SDO						
I_{LEAK}	Input leak current	Under working/sleeping mode, connected with VDD		13.4		mA
		Under working/sleeping mode, connected with GND	-1	-	1	uA
		Under working/sleeping mode, connected with 1.5V		12.72		mA
		Under working/sleeping mode, unconnected	-1	-	1	uA
V_{OH}	Output voltage high level	VDD(PVDD)=3V; IO=4mA	VDD(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	VDD(PVDD)=3V; IO=4mA	VSS(PVSS)	-	V_{SS}(PVSS)+0.4	V
MFOUT, IRQ						
I_{LEAK}	Input leak current		-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V

V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	VDD(PVDD)=3V; IO=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	VDD(PVDD)=3V; IO=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V
I_{OH}	High level output current	VDD(PVDD) = 3 V	-8.5		-7.3	mA
I_{OL}	Low level output current	VDD(PVDD) = 3 V	7.3		8.5	mA
OSCOUT						
I_{LEAK}	Input leak current	Under working mode, connected with VDD		8.01		mA
		Under working mode, connected with GND		2.49		mA
		Under working mode, connected with 1.5V		3.3		mA
		Under working mode,unconnected	-1	-	1	uA
I_{LEAK}	Input leak current	Under sleeping mode, connected with VDD		8.35		mA
		Under sleeping mode, connected with GND	-1	-	1	uA
		Under sleeping mode, connected with 1.5V		3.7		mA
		Under sleeping mode,unconnected	-1	-	1	uA
V_{IH}	Input voltage high level		0.7PVDD			V
V_{IL}	Input voltage low level				0.3PVDD	V
V_{OH}	Output voltage high level	V_{DD}(PVDD)=3V; I_O=4mA	V_{DD}(PVDD)-0.4	-	V_{DD}(PVDD)	V
V_{OL}	Output voltage low level	V_{DD}(PVDD)=3zxsV; I_O=4mA	V_{SS}(PVSS)	-	V_{SS}(PVSS)+0.4	V

Pinouts of QFN32



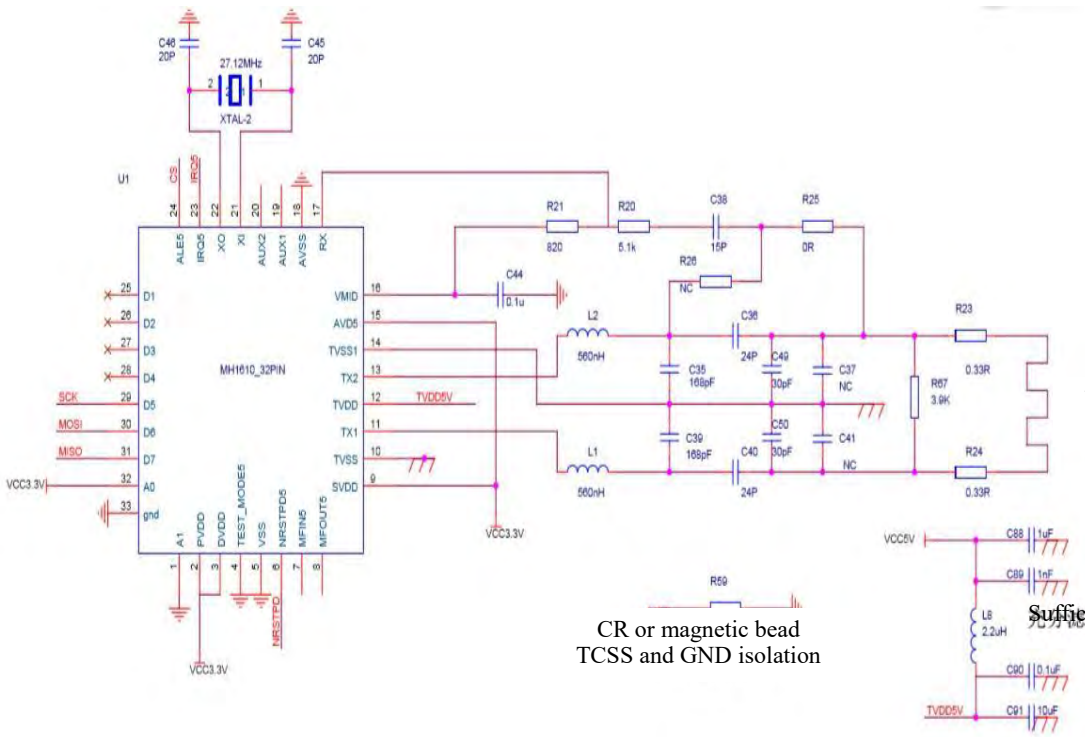
Pin configuration QFN32

Pin Description of QFN32

S/N	Symbol	Type	Description
1	I2C	I	I2C Interface enabling
2	PVDD	PWR	Pin power supply
3	DVDD	PWR	Digital power
4	DVSS	PWR	Digital ground
5	PVSS	PWR	Pin power ground
6	NRSTPD	I	Reset or power-down pin, active low
7	MFIN	I	Signal input
8	MFOUT	O	Signal output

9	SVDD	PWR	Power supply of MFIN and MFOUT
10	TVSS	PWR	Ground of transmitter
11	TX1	O	Transmission of modulated energy carrier signal of 13.56MHz
12	TVDD	PWR	Power supply of transmitter
13	TX2	O	Transmission of modulated energy carrier signal of 13.56MHz
14	TVSS	PWR	Ground of transmitter
15	AVDD	PWR	Analog power supply
16	VMID	PWR	Internal reference voltage
17	RX	I	Signal input
18	AVSS	PWR	Analog ground
19	AUX1	O	Test pin
20	AUX2	O	Test pin
21	OSCIN	I	Externally connect with 27.12MHz crystal or clock signal.
22	OSCOUT	O	Externally connect with 27.12MHz crystal
23	IRQ	O	Output interruption signal
24	SDA/NSS/RX	I/O	Communication interface of SPI/I2C/UART/ parallel port
25	D1/ADR_5	I/O	
26	D2/ADR_4	I/O	
27	D3/ADR_3	I/O	
28	D4/ADR_2	I/O	
29	D5/ADR_1/SCK	I/O	
30	D6/ADR_0/MOSI	I/O	
31	D7/SCL/MISO/TX	I/O	
32	EA	I	Encoding I2C address

Schematic diagram of typical SPI communication



Typical periphery

Note:

[1] The read-write distance of MIFARE card can be reached to 9cm. The distance is affected by the antenna size and the tuning specifically.

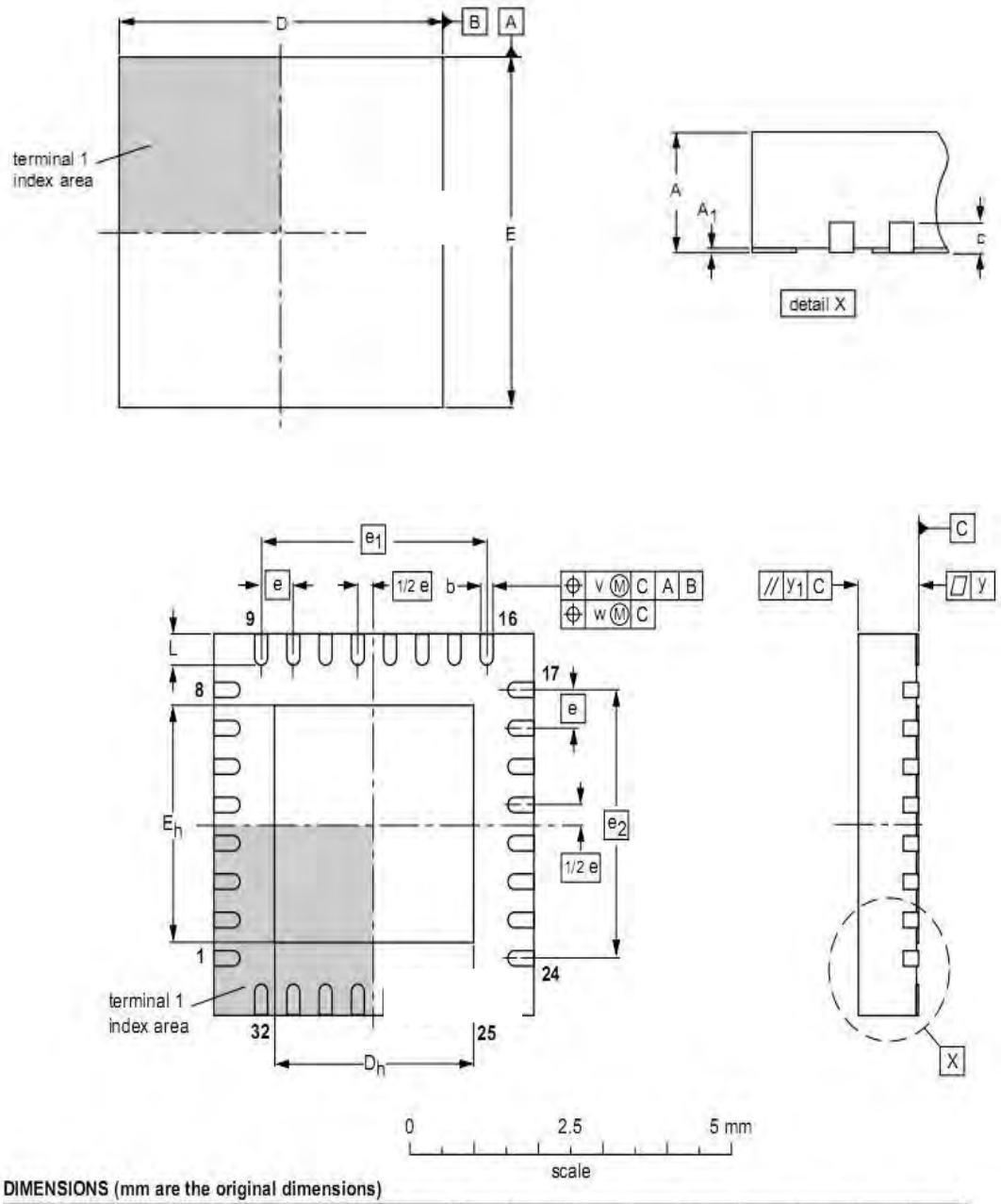
[2] TVSS and GND must be sufficiently isolated.

[3] Power supplies of TVDD, AVDD, SVDD and DVDD need to be sufficiently isolated.

[4] The peripheral matching needs to be re-adjusted based on different antenna designs.

[5] The value of R67 is expected to be adjusted during the EMV3.1 certification test.

Package Outline



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

QFN32 package outline

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